4th Generation Intel® Core™ Processor, codenamed Haswell

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Sequence

Family of Innovations!

Power Efficiency and Management

FIVR – Fully Integrated Voltage Regulator

Cache Hierarchy and Interconnects

Gfx/Media

Intel® Microarchitecture (Haswell): Core

ISA

Wrap Up
Family of Innovations

- **Huge family**: SOC methodology, common architecture
- **Low power platform**: 20x idle power reduction, low power IO (I2C, SDIO, I2S, UART), Link power management (USB, PCIe, SATA)
- **Large eDRAM Cache**
- **Platform**: PSR (Panel Self Refresh)
- **FIVR**: Fully Integrated Voltage Regulator
- **Core**: FMA (Floating-point Multiply Add), 2x Cache BW, TSX (Transaction Synchronization Extension)
- **Graphics**: 2x in Ultrabooks, OpenCL 1.2, DX 11.1, OpenGL 4.0
- **Media**: 5x faster at 0.5x power

Modularity Options

<table>
<thead>
<tr>
<th>Value</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Count</td>
<td>2-4</td>
</tr>
<tr>
<td>Graphics</td>
<td>GT1, GT2, GT3</td>
</tr>
<tr>
<td>Active Power Level</td>
<td>Tablet to Desktop</td>
</tr>
<tr>
<td>Idle Power</td>
<td>Variable</td>
</tr>
<tr>
<td>Cache Size</td>
<td>Variable</td>
</tr>
<tr>
<td>Interconnects</td>
<td>Variable</td>
</tr>
<tr>
<td>Platforms</td>
<td>Traditional, power optimized</td>
</tr>
</tbody>
</table>

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# Intel Process 22nm Process Technology and Tick/Tock Development Model

## Enhanced version of Intel’s 22nm Process Technology
- 22nm Tri-Gate transistors enhanced to reduce leakage current 2-3X with the same frequency capability
- Haswell version of 22nm has 11 metal interconnect layers compared to 9 layers on Ivy Bridge to optimize performance, area and cost

## Haswell builds on innovations in 2nd and 3rd Generation Intel® Core™ i3/i5/i7 Processors (Sandy Bridge/Ivy Bridge) with optimized Intel process technology!
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Wrap Up
Power Efficiency: Maximizing Power-Limited Performance

- Extended operating range
  - Increased Turbo
  - New C-states, improved latency
  - Power efficient features: better than voltage / frequency scaling
  - Continued focus on gating unused logic and low-power modes
  - Optimized manufacturing and circuits

- Independent frequency domains
  - Cores separated from LLC+Ring for fine-grained control
  - Power Control Unit dynamically allocates budget when power-limited
  - Prioritization based on run-time characteristics selects domain with the highest performance return
Haswell Power Management Innovation

• All day experiences
  – Improving power efficiency for active workloads

• Evolutionary improvements

• New extremely low-power active state
  – 20x improvement from prior generation
  – Enables significant improvement in realizable battery life
  – Automatic, continuous, fine-grained, transparent to well written SW
  – Leverages learnings from phone & tablet development

**Everything that is not needed is turned off!**

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Wrap Up
Ivy Bridge Platform

- Core VR variable voltage: 0V-1.2V
- Graphics VR variable voltage: 0V-1.2V
- System agent VR
- PLL VR 1.8V

Haswell Platform

- Haswell Processor
- FIVR VRs:
  - Vccsa
  - Vccio
  - Vccioa
  - VccCore 0
  - VccCore 1
  - VccCore 2
  - VccCore 3
  - VccCache
  - Graphics0
  - Graphics1
  - VccEDRAM
  - VccOPIO

- Logic Blocks

Example voltage planes
FIVR: Platform Goodness

Ivy Bridge
- Back is all power
- Large inductors, butterfly mounted through board
- 5.4mm thick

Haswell
- Backside bare
- Small inductors & caps & 75% fewer
- Space for 10% larger battery
- 3.4mm thick

2mm thinner; ~$5 cheaper; space for 10% larger battery
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Cache Hierarchy and Interconnects
Gfx/Media
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Wrap Up
Cache, Interconnect and System Agent

• More access bandwidth per slice of shared LLC
  – New dedicated pipelines handle data and non-data accesses independently

• Improved load balancing to System Agent
  – Better credit-based management more efficiently shares resources

• Improved DRAM write throughput
  – Deeper pending queues: more decoupling, better scheduling

• Lower power, better efficiency
  – Focused effort to reduce idle and active power (next section)
Large eDRAM Cache

- Haswell introduces configurations with large graphics & large cache
- Cache attributes
  - High throughput and low latency
  - Flat latency vs. sustained bandwidth curve
  - Fully shared between Graphics, Media, and Cores for very efficient multi-media computing
Large Caches in Graphics Workloads

- **Intra-frame**
  - Intra-render pass – capture spatial and temporal locality within a surface
    - Captured in moderate cache sizes (1-8MB LLC). SNB Si shows 20-30% speedup
  - Inter-render pass – capture a full surface from generation to subsequent consumption (shadow maps, render targets)
    - Captured in big cache sizes (16-64+MB LLC). CRW Si shows 20-30% speedup

- **Inter-frame**
  - Capture texture reuse across frames due to continuity between frames
Large Cache Performance and Latency

Small latency sensitivity with load. Sustainable for random traffic.

Pre-production system measurements, product measurements may vary.

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Wrap Up
Haswell Processor Graphics Architecture Building Blocks

Scalable Architecture partitioned into 6 domains:

1. Global Assets: Geometry Front-end up to Setup
2. Slice Common: Rasterizer, Level 3 Cache (L3$) and Pixel Back-end
3. Sub-Slice: Shaders (EUs), Instruction Caches (IC$) and Samplers
   - Scalable slices for performance and GFlop tuning
4. Multi-Format Video CODEC Engine (MFX)
5. Video Quality Enhancement Engine
6. Displays

Sets the stage for Scale-up!!
Video Codec

Introducing hardware-based SVC (Scalable Video Coding) codec
- Allowing single encoded bit-stream for heterogeneous devices
- Key enabler for multi-participant video conferencing

MJPEG (Motion JPEG) hardware decoder
- Enabling low power HD video conferencing for USB2 webcam

MPEG2 hardware encoder
- DVD creation
- DLNA streaming

4Kx2K video playback
Continue to drive encoder quality
- Introduced through the encoding modes in Media SDK

Haswell adds newer codec on top existing codecs in 3rd Generation Intel® Core™ processors
High Quality Video Processing

Dedicated video processing on newly designed Video Quality Engine (VQE)

Haswell supports an extensive suite of video processing functions including:

- De-Noise (DN)
- De-Interlace (DI)
- Film-mode Detection (FMD)
- Skin Tone Detection (STD)
- Skin Tone Enhancement (STE)
- Total Color Control (TCC)
- Adaptive Contrast Enhancement (ACE)
- Advanced Video Scalar (AVS)
- Gamut Compression (GC)
- Gamut Expansion (GE)
- Skin Tone Tuned Image Enhancement Filter
- Frame Rate Conversion (FRC)
- Image Stabilization (IS)

1New on Haswell

Higher quality video at lower power!
Media: Quick Sync Video Performance and Power

- 4-12x real-time transcode at various quality modes
- 10-hour video playback time on latest Apple MacBook Air
- Multi-stream 4K decode
- > real-time 4K Encode

*Measurements based on Intel Demo Clip in Cyberlink Media Espresso Fast Conversion Mode

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Wrap Up
Haswell Core at a Glance

Next generation branch prediction
• Improves performance and saves wasted work

Improved front-end
• Initiate TLB and cache misses speculatively
• Handle cache misses in parallel to hide latency
• Leverages improved branch prediction

Deeper buffers
• Extract more instruction parallelism
• More resources when running a single thread

More execution units, shorter latencies
• Power down when not in use

More load/store bandwidth
• Better prefetching, better cache line split latency and throughput, double L2 bandwidth
• New modes save power without losing performance

No pipeline growth
• Same branch mis-prediction latency
• Same L1/L2 cache latency
## Haswell Buffer Sizes

Extract more parallelism in every generation

<table>
<thead>
<tr>
<th></th>
<th>Nehalem</th>
<th>Sandy Bridge</th>
<th>Haswell</th>
</tr>
</thead>
<tbody>
<tr>
<td>Out-of-order Window</td>
<td>128</td>
<td>168</td>
<td>192</td>
</tr>
<tr>
<td>In-flight Loads</td>
<td>48</td>
<td>64</td>
<td>72</td>
</tr>
<tr>
<td>In-flight Stores</td>
<td>32</td>
<td>36</td>
<td>42</td>
</tr>
<tr>
<td>Scheduler Entries</td>
<td>36</td>
<td>54</td>
<td>60</td>
</tr>
<tr>
<td>Integer Register File</td>
<td>N/A</td>
<td>160</td>
<td>168</td>
</tr>
<tr>
<td>FP Register File</td>
<td>N/A</td>
<td>144</td>
<td>168</td>
</tr>
<tr>
<td>Allocation Queue</td>
<td>28/thread</td>
<td>28/thread</td>
<td>56</td>
</tr>
</tbody>
</table>
**Haswell Execution Unit Overview**

**Unified Reservation Station**

- Port 0: Integer ALU & Shift
- Port 1: Integer ALU & LEA
- Port 2: Load & Store Address
- Port 3: Store Data
- Port 4: Integer ALU & LEA
- Port 5: Integer ALU & Shift
- Port 6: Store Address
- Port 7: Store Address

- **FMA FP Multiply**: Doubles peak FLOPs, benefits legacy
- **FMA FP Add**: Benefits legacy
- **Vector Int Multiply**: For vector workloads
- **Vector Int ALU**: For vector workloads
- **Vector Logicals**: For vector workloads
- **Branch**: Reduces Port0 Conflicts
- **Divide**: For floating-point division
- **Vector Shifts**: For vector shifts

- **4th ALU**: Great for integer workloads, frees Port0 & 1 for vector

- **2xFMA**
  - Doubles peak FLOPs
  - Two FP multiplies

- **New Branch Unit**
  - Reduces Port0 Conflicts
  - 2nd EU for high branch code

- **New AGU for Stores**
  - Leaves Port 2 & 3 open for Loads

Intel® Microarchitecture (Haswell)
FMA (Floatingpoint Multiply Add)

- 2 new FMA units provide 2x peak FLOPs/cycle of previous generation
- 2X cache bandwidth to feed wide vector units
  - 32-byte load/store for L1
  - 2x L2 bandwidth
- 5-cycle FMA latency same as an FP multiply

FMA provides improved accuracy and performance

<table>
<thead>
<tr>
<th>Latency (clks)</th>
<th>Prior Gen</th>
<th>New Haswell</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>MulPS, PD</td>
<td>5</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>AddPS, PD</td>
<td>3</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Mul+Add /FMA</td>
<td>8</td>
<td>5</td>
<td>1.6</td>
</tr>
</tbody>
</table>
## Core Cache Size/Latency/Bandwidth

<table>
<thead>
<tr>
<th>Metric</th>
<th>Nehalem</th>
<th>Sandy Bridge</th>
<th>Haswell</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1 Instruction Cache</td>
<td>32K, 4-way</td>
<td>32K, 8-way</td>
<td>32K, 8-way</td>
</tr>
<tr>
<td>L1 Data Cache</td>
<td>32K, 8-way</td>
<td>32K, 8-way</td>
<td>32K, 8-way</td>
</tr>
<tr>
<td>Fastest Load-to-use</td>
<td>4 cycles</td>
<td>4 cycles</td>
<td>4 cycles</td>
</tr>
<tr>
<td>Load bandwidth</td>
<td>16 Bytes/cycle</td>
<td>32 Bytes/cycle (banked)</td>
<td>64 Bytes/cycle</td>
</tr>
<tr>
<td>Store bandwidth</td>
<td>16 Bytes/cycle</td>
<td>16 Bytes/cycle</td>
<td>32 Bytes/cycle</td>
</tr>
<tr>
<td>L2 Unified Cache</td>
<td>256K, 8-way</td>
<td>256K, 8-way</td>
<td>256K, 8-way</td>
</tr>
<tr>
<td>Fastest load-to-use</td>
<td>10 cycles</td>
<td>11 cycles</td>
<td>11 cycles</td>
</tr>
<tr>
<td>Bandwidth to L1</td>
<td>32 Bytes/cycle</td>
<td>32 Bytes/cycle</td>
<td>64 Bytes/cycle</td>
</tr>
<tr>
<td>L1 Instruction TLB</td>
<td>4K: 128, 4-way</td>
<td>4K: 128, 4-way</td>
<td>4K: 128, 4-way</td>
</tr>
<tr>
<td></td>
<td>2M/4M: 7/thread</td>
<td>2M/4M: 8/thread</td>
<td>2M/4M: 8/thread</td>
</tr>
<tr>
<td>L1 Data TLB</td>
<td>4K: 64, 4-way</td>
<td>4K: 64, 4-way</td>
<td>4K: 64, 4-way</td>
</tr>
<tr>
<td></td>
<td>2M/4M: 32, 4-way</td>
<td>2M/4M: 32, 4-way</td>
<td>2M/4M: 32, 4-way</td>
</tr>
<tr>
<td></td>
<td>1G: fractured</td>
<td>1G: 4, 4-way</td>
<td>1G: 4, 4-way</td>
</tr>
<tr>
<td>L2 Unified TLB</td>
<td>4K: 512, 4-way</td>
<td>4K: 512, 4-way</td>
<td>4K+2M shared: 1024, 8-way</td>
</tr>
</tbody>
</table>

All caches use 64-byte lines

Intel® Microarchitecture (Haswell); Intel® Microarchitecture (Sandy Bridge); Intel® Microarchitecture (Nehalem)
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Wrap Up
Haswell New Compute Instructions

Intel® Advanced Vector Extensions 2 (Intel® AVX2)

• Includes
  – 256-bit Integer vectors
  – FMA: Fused Multiply-Add
  – Full-width element permuters
  – Gather
• Benefits
  – High performance computing
  – Audio & Video
  – Games
• New Integer Instructions
  – Indexing and hashing
  – Cryptography
  – Endian conversion – MOVBE

• Full Instruction Specification Available at: http://software.intel.com/en-us/avx/

<table>
<thead>
<tr>
<th></th>
<th>Instruction Set</th>
<th>SP FLOPs per cycle</th>
<th>DP FLOPs per cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nehalem</td>
<td>SSE (128-bits)</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>Sandy Bridge</td>
<td>AVX (256-bits)</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>Haswell</td>
<td>AVX2 &amp; FMA</td>
<td>32</td>
<td>16</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Group</th>
<th>Instructions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit Field Pack/Extract</td>
<td>BZHI, SHLX, SHRX, SARX, BEXTR</td>
</tr>
<tr>
<td>Variable Bit Length Stream Decode</td>
<td>LZCNT, TZCNT, BLSR, BLSMSK, BLSI, ANDN</td>
</tr>
<tr>
<td>Bit Gather/Scatter</td>
<td>PDEP, PEXT</td>
</tr>
<tr>
<td>Arbitrary Precision Arithmetic &amp; Hashing</td>
<td>MULX, RORX</td>
</tr>
</tbody>
</table>
Cryptography protects nearly all data and transactions you want to keep secure.

SHA-256:
- AVX2 - Wider
- Multibuffer
- PCLMULQDQ

RSA 2048:
- MULX - Multiply

AES GCM:
- AES-NI

Haswell’s microarchitecture improvements and new instructions enable substantial gains in cryptography.

SHA-256:
- RORX – Rotates, AVX2
Locks!

HLE: Hardware Lock Elision – XACQUIRE/XRELEASE

- Software uses legacy compatible hints to identify critical section. Hints ignored on hardware without TSX.
- Hardware support to execute transactionally without acquiring lock
- Abort causes a re-execution without elision
- Hardware manages all architectural state

RTM: Restricted Transactional Memory – XBEGIN/XEND

- Software uses new instructions to specify critical sections
- Similar to HLE but flexible interface for software to do lock elision
- Abort transfers control to target specified by XBEGIN operand
- Abort information returned in a general purpose register (EAX)

XTEST and XABORT – Additional instructions

Bringing Transactional Memory to the Mainstream
Substitute atomic operations, locks, and non-blocking sync. with RTM

• Average 1.41x speedup with 8 threads

Workloads benefit from RTM by

1. Exploiting concurrency within a critical section (**nufft**)
2. Reducing the synchronization cost (**ssca2, physicsSolver, nufft, histogram**)
3. Replacing complex non-blocking sync. w/ regular memory ops (**canneal**)

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Virtualization on Haswell with Intel® VT

Substantially improved guest/host transition times

New *Accessed* and *Dirty* bits for Extended Page Tables (EPT) eliminates major cause of vmexits

Overhauled TLB invalidations – lower latency, less serialization

New VMFUNC instruction enables hyper-calls without a vmexit

Intel® VT-d adds 4-level page walks to match Intel® VT-x

Haswell reduces round-trip to <500 cycles

Intel VT-x Roundtrip over Generations
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