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Topics

X-Gene  ▪ Roadmap

X-Gene1 ▪ Review
  ▪ Design targets
  ▪ Architecture

X-Gene2 ▪ Changes from X-Gene1
  ▪ Integrated RoCE HCA
  ▪ Performance

X-Gene3 ▪ Features
### X-Gene: Product Roadmap

**X-Gene 1**  
40nm  
- 8 Core, 2.4GHz  
- 4 channels memory  
- 2x 10G NIC  

**X-Gene 2**  
28nm  
- 8-16 Core, 2.4-2.8GHz  
- 4 channels memory  
- Low latency RoCE, for cloud and HPC workloads  

**X-Gene 3**  
16nm FINFET  
- Large core count, 3GHz  
- 2nd gen RoCE  
- 2015

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**In Production**  
**Sampling**  
**In Design**
X-Gene1 (Storm)

- First generation ARMv8 CPU
- 8 Cores 2.4GHz
- 8MB L3 cache
- 4 DDR memory channels
- PCIE Gen3
- SATA Gen3
- 1/10G interfaces
- Integrated NIC
- 40nm TSMC
- System management
- Security, networking and scale-out accelerators
X-Gene 1 Products

X-Gene ARM Servers are here!
What Are Scale-out Applications

What are scale-out applications?
Pretty much anything that runs in the datacenter today:

- **Web Front End** — Large scale web services hosting
- **Web Search** — Index serving, data harvesting
- **Data serving** — NoSQL data storage and retrieval
- **Data analytics** — Information classification, filtering and extraction
- **Media serving** — Large scale hosting and streaming of content

- **They run on 1000s of CPUs. 2P/4P/8P processors do not matter**
- **Communication b/w Application Threads is the bottleneck (Latency, BW)**

**Thread resources matter**
- Memory/Thread
- Memory BW/Thread
- CacheSize/Thread
- IO Throughput/Thread
- Storage Capacity/Thread

**Application latency**
- 100s of microseconds
- TCP/IP as an example:
  - Multiple buffer copies
  - Chatty handshake
  - High s/w overhead
Why RoCE (RDMA over Converged Ethernet)?

- Target the rack level first
  - Let’s not change the world .. Yet!
- Use existing switching infrastructure
  - Ethernet is the incumbent
  - Let’s not change the link layer
- Reduce latency where it matters
  - Reduce 500ns to 100ns?
  - Or reduce 50us to 4us?
  - Take care of the end-end latency rather than each hop
- Take advantage of existing software infrastructure
  - Standard API interfaces
  - Existing libraries
  - Existing infrastructure

<table>
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<tr>
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<th>10G Ethernet</th>
<th>10G RoCE</th>
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<td>Latency Reduction</td>
<td>1X</td>
<td>6X</td>
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<tr>
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<td>1X</td>
<td>4X</td>
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X-Gene2 Target

- Design for the rack-level
- Optimize the performance of each application thread
  - OOO, 4-issue, 2.8GHz CPU
  - High memory b/w per thread
  - High IO and Storage b/w per thread
- Design the most efficient application interconnect for these CPUs
- Application interconnect that works not just for 2P/4P, but for hundreds of CPUs
- Reduce application latency by a magnitude of 10
  - RoCE: 40us → 5us
- Improve rack level performance at a given latency by 2-3X
X-Gene2 CPU target

**CPU Performance**

- **IIW:** Instruction Issue Width
- **IO:** Instruction Issue
- **CH:** Cache Hierarchy
- **C/CPU:** Cache per CPU
- **M/CPU:** Memory Bandwidth/CPU

**X-Gene2**

- **IIW:** 4issue
- **IO:** OOO
- **CH:** 3 level
- **CpC:** >2400KB
- **MpC:** 7.5GB/s
- **Freq:** 3.3GHz

- **IIW:** 2issue
  - **IO:** In-Order
  - **CH:** 2 level
  - **CpC:** 400KB
  - **MpC:** 1.2GB/s
  - **Freq:** 1.8GHz

- **IIW:** 3issue
  - **IO:** OOO*
  - **CH:** 3 level
  - **CpC:** 1200KB
  - **MpC:** 3.2GB/s
  - **Freq:** 2.4GHz

- **IIW:** 2issue
  - **IO:** OOO*
  - **CH:** 2 level
  - **CpC:** 568KB
  - **MpC:** 3.2GB/s
  - **Freq:** 2.4GHz

- **IIW:** 3issue
  - **IO:** OOO*
  - **CH:** 3 level
  - **CpC:** 1600KB
  - **MpC:** 3.2GB/s
  - **Freq:** 2.4GHz

- **IIW:** 4issue
  - **IO:** OOO
  - **CH:** 3 level
  - **CpC:** >2400KB
  - **MpC:** 7.5GB/s
  - **Freq:** 3.3GHz

**Cost**
- Second generation ARMv8 CPU
- 8 Cores 2.8 GHz
- 8MB L3 cache
- 4 DDR channels
- PCIE Gen3
- SATA Gen3
- 1/10G interfaces
- Integrated NIC
- 28nm TSMC
- System management
- Security, networking and cloud accelerators
- Integrated RoCE HCA
- NFV (OVS) and SDN support
X-Gene™ Processor Module

Processor Module
- 2 cores + shared L2 cache
- 4 wide out-of-order superscalar microarchitecture
- >100 instructions in flight
- Integer, scalar, HP/SP/DP FPU and 128b SIMD engine
- Hardware virtualization support
- Hardware tablewalk and nested page tables
- Full set of static and dynamic power management features
  - Fine grain/macro clock gating, DVFS
  - C0, C1, C3, C4, C6 states

Cache Hierarchy
- Separate L1I and L1D caches
- Shared L2 cache among 2 CPUs
- Last-level globally shared L3 Cache
- Advanced hardware prefetch in L1 and L2
- L2 inclusive of L1 write-thru data caches

RAS
- ECC and Parity protection of all Caches, Tags, TLBs
- Data poisoning and error isolation
X-Gene2 CPU Block Diagram

From L2 Cache

- BTB
- Ret Stk
- CBr Pred

- Instr Cache
- Instr Buf

- Instr Group (4x)
- Instr Dec / Xlat (4x)
- Rename (4x)

- Global Pipe Ctrl
  - BrChkptBuf
  - OpChkptBuf

- IXU Op InputBuf
  - Branch Sched
  - Branch Pipe
  - IXU Sched
  - Simple Int Pipe
  - Complex Int Pipe

- Load Sched
- Load Pipe

- Store Sched
- Store Pipe

For L2 Cache

- MMU
- L2 TLB
- Data Cache
- WCQ

- SDB / SFB

- FSU
  - Op Buf
  - Ld Data Buf
  - Floating Point / SIMD Pipe
  - FpSimd Sched
  - St Data Buf

- IXU Op InputBuf
- Op InputBuf
- Op InputBuf

- Clk & Pwr Management
- Debug / Trace
- Interrupt Control
- Timers
X-Gene2 Instruction Fetch

I-Cache & Fetch Unit
- Reduced Vmin RAMs
- Larger branch predictors
  - BTB size doubled
  - CBP size doubled
  - IBP size quadrupled
X-Gene2 Reorder Buffer, Dispatch and Control

Pipeline Control
Higher trace compression
Finer-grain clock throttling
X-Gene2 Integer, Branch, Load and Store Units

- Integer and Load/Store Units
  - Increased branch and integer scheduler entries

- Debug/Trace
- Interrupt Control
- Timers
- Clk & Pwr Management

- Branch Sched
- IXU Sched
- Load Sched
- Store Sched

- Branch Pipe
- Simple Int Pipe
- Simple/Complex Int Pipe
- Load Pipe
- Store Pipe
Data Cache

- Reduced Vmin RAMs
- Improved instruction and data prefetchers
  - Support for more streams
  - Support for larger stride patterns
Design Challenges from Device Variation

- Impact of device variation is increased in newer technology and increase in transistor count
  - Channel Length may vary due to lithography and optical defects or deviations during etch
  - Vt may vary due to dopant fluctuations or irregularities from the annealing process
  - Oxide thickness variation due to surface roughness scattering

- Additional considerations for process variation required beyond design margining and corner analysis
  - High sigma variation on sensitive gates can dominate a timing path in high frequency designs
  - High number of timing paths lead to an increased likelihood of variation-based outlier paths lowering design frequency
  - Design robustness in memory designs require statistical analysis
Techniques to address device variation

- **P&R level**
  - Traditional corner analysis over wide PVT range
  - Design specific OCV margining
  - Cell-based voltage and process sensitivity analysis for top timing paths, which covers thousands of timing paths
  - Usage screening and extensive analysis on hold fixing cells

- **Device level**
  - Traditional corner analysis over wide PVT range
  - Extensive statistical analysis on all ratio-ed logic, then optimized to obtain near normal distribution
  - Statistical analysis with voltage variance on clock distribution network to limit worst case skew and duty-cycle jitter
  - Device variation optimization on all critical memory timing paths, either with selected devices or carved extraction
RoCE Features in X-Gene2

- Verbs Interface compliant
- RDMA over Converged Ethernet
- Hardware-based RC Transport – SRQ support
- RDMA, SEND and ATOMIC operations
- MTU sizes of 256B, 512B, 1KB

- 2 Ports of 10GE
- Large burst of 64B packets and wire-speed processing for < 128B packets
- Along with standard GID, APM specific routable RoCE options

Latency reduction from 50us to 5us compared to TCP/IP
X-Gene2 High Density Rack

- 42U
- 6480 2.8GHz Application Threads
- 50TB Memory, 48TB/s Memory b/w
  - RoCE interconnect b/w CPUs
- Shared Storage and IO
- 750M TPS* (X-Gene2)
- vs. 400M TPS* (Current Server, equiv power)

*TP95 @40ms Memcached
X-Gene2 Performance

**Spec2006_rate/W**

- SpecIntRate2006_Peak w gcc –O3
- Power: TDP

**Memcached TPS @30us**

**ApacheBench**

- Performance measured running Apache Web server 2.4.x
- 16KB File request size, 400 concurrent flows
X-Gene3 (Skylark)

- Third generation ARMv8 CPU
- Further micro-architecture enhancements to X-Gene2
- 16-64 Cores 3GHz
- Inter-rack interconnect
- 16nm FinFET
- 2015 samples