OpenPOWER: Reengineering a server ecosystem for large-scale data centers

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OpenPOWER is about choice in large-scale data centers

**The choice to differentiate**
- build workload optimized solutions
- use best-of-breed components from an open ecosystem

**The choice to innovate**
- collaborative innovation in open ecosystem
- with open interfaces

**The choice to grow**
- delivered system performance
- new capabilities instead of technology scaling
Competing Forces Are Shaping the Data Center Landscape

Need for Standardization

Economies of Scale Enable Data Center Optimization

Need for Innovation

Reduction in Choice for Data Center Operators and Vendors

Hardware Development
- Consumer Scale Volumes
- DIY servers

Software Development
- Known Software Stack
- Higher Programmer Productivity

“X86 Everywhere”

Hardware Development
- Optimize for Servers
- Increase Value & Differentiation

Software Development
- Portability & Platform Choice
- Workload Optimization

One Size Does Not Fit All
OpenPOWER unchains scale out data centers

- A consortium of data center suppliers and operators
- Jointly create vibrant open ecosystem for data centers
- Expand options for large-scale data center computing
- Software stacks as true measure of ecosystem
OpenPOWER ecosystem framework

- Enable rich ecosystem of hardware vendors
  - Standardized hardware interfaces
  - Common, open firmware interfaces

- Open source system software stack
  - Data center operators rely on tuning SW stack
  - Enable server ODM vendors to create offerings
  - Operating environment built on Linux and KVM

- Simplify porting of scale-out data center applications
  - Application source code dependences
  - In-storage data base formats
  - Exploit I/O and accelerators originally designed for PCs
  - Little-endian data format and programming interfaces
A new Open Power Linux environment

- OpenPOWER is not the traditional Power Linux with a new name
  - Significant discontinuity and fresh start
  - No Binary Compatibility to Legacy Power Linux
    ⇒ new environment “ppc64le”
  - New: Firmware, Hypervisor, data layout, source code, ELFv2 ABI

- What changes for application developers?
  - Byte order
  - New ABI
  - Vector programming API

- Extremely rapid turn-around from decision to develop to deployment
  - First discussions in March 2013, Linux distro builds starting October 2013
  - >40000 packages built within short time
The New OpenPOWER Application Binary Interface (ABI)

• Starting point: PPC64 / AIX ABI
  – Established, tested production code
  – Commonality and maintenance across LE, BE and AIX where feasible
  – Minimum disruption for tooling: GCC, XL, Java, LLVM, libffi, PyPy, …

• Define new capabilities as delta over baseline
  – Align with the broader ecosystem
  – Create hardware optimization opportunities / synergies
  – Optimize for modern code patterns
    More classes, abstraction
    Shorter function lengths
    More indirect calls

• **If it ain’t broken, don’t fix it!**
Optimizing Data Access with the Global Offset Table (GOT)

- Initialize pointer to GOT without functions descriptors
  - Dual entry points to re-use GOT on local call

- Optimize GOT pointer update on cross-module calls
  - Schedule GOT pointer save in caller

- Expand addressing range with “Medium Code Model”
  - Exploit Fusion and avoid GOT overflow code

- Optimize GOT in main module
  - Generate non-PIC code and resolve symbols at link time
Global Offset Table (GOT)

- Global Offset Table: data dictionary
  - Holds addresses for global data

- The GOT pointer points to data dictionary
  - load data address for indirect access (GOT-indirect)
  - load data directly (GOT-relative)

- Each module (shared library) has a different GOT
  - Cross-module calls save/restore old and load new GOT pointer
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Establishing the GOT pointer

- Two entry points for each function
  - “Local EP”: shared GOT in same module
  - “Global EP”: initialize new GOT for module
  - Symbol table points to Global EP

- Direct call provides current GOT pointer (in r2)
  - Linker resolves local call to Local EP
  - Linker resolves extern call to PLT stub
    - Extern call resolved by dynamic linker
    - PLT stub performs indirect call to function

- Indirect calls to Global EP
  - Function entry address in r12

```c
f(char *buf) {
    puts(buf);
}
```
Optimizing GOT pointer save and restore

• Compiler collaborates with linker
  – Reduce GOT management overhead

• Optimizing placement of GOT pointer save points for external calls
  – Compiler schedules a placeholder for a GOT pointer save
  – Static linker populates placeholder with GOT save instruction if and only if an external function call is made
Call cost reduction with scheduled GOT store

- Remove repeated store of GOT pointer
- Avoid forwarding of in-flight store to dependent load
Medium Code Model

• “Medium code model” addresses growing data size
  – Expand GOT data dictionary to up to 4GB
  – Memory access with 32b displacement

• The size of the data dictionary is constrained by displacement range
  – Fixed width RISC ISA constrains the displacement to 16b
    • 64KB “natural” dictionary size (8k variables)
  – Dictionary overflow handling can penalize performance

• “Medium Code Model” as default: facilitate organic application growth
  – Enable applications to grow beyond 8K to 500M variables per module
  – “Beyond RISC” using Displacement Fusion capability in Power8
Beyond RISC: Displacement Fusion

• “Fusion” allows processor to build **internal compound instruction**
  – Combine multiple instructions into internal compound instruction
  – CISC addressing range while retaining RISC fixed-width advantage

• Compound instruction executes as a single hardware operation
  – Fewer resources, shorter latency
  – Improved performance for programs with large data sets

```
addis r3=r2, D1@ha
ld r3=r3, D1@l

Displacement fusion

ld r3= r2, D1
```

```
addis r3 | r2  | high(D1)  
ld     r3 | r3  | D1

internal compound instruction

ld r3 | r2  | D1
```
Function Call Improvements

• Parameter passing
  – Pass/return more parameters in registers

• Streamline stack frame
  – Allocate parameter save area only when required

• More descriptive object file info
  – More precise DWARF, Reloc’s, and ELF format flags
  – Improve future ABI extensibility
Register usage for function arguments

- Goal: Reduce abstraction penalty ("same performance as builtin types")
  - OO languages wrap basic data types in a class
  - Previous Power ABI passes most classes via GPRs
  - ... and returns most class results in memory
    - Other common ABIs pass and return class in memory

- Goal: Pass each data type in "natural" register
  - Integer parameters ➔ general purpose registers
  - Floating point parameters ➔ floating point registers
  - Vector parameters ➔ vector registers
Register usage for function arguments

• Pass more class types as register parameters
  ⇒ Solution: homogeneous float/vector aggregates
  – Up to 8 members passed in natural registers

• Return function results in same register(s) as first input parameter
  – Aggregates returned in multiple registers
  – Homogenous float and vector aggregates in float and vector registers

• Significant improvement for abstract data type handling
  – 3x-4x performance improvement for invocations of class vertex<float>
  – Class std::complex<> matches native _Complex type performance
  – ~1%-5% performance improvement for many OO codes
ABI performance

• Unchanged performance in programs with
  – Large functions / subroutines
  – Extensive inlining

• Faster performance in programs with:
  – Large GOT with many global variables
  – Calls to small functions
  – Pointer calls including virtual function calls.
  – Functions with abstract data types
  – ...
OpenPOWER Vector SIMD Programming Model

• Transcends traditional hardware-centric SIMD programming models
  – Vector SIMD API describes *what* SIMD processing to perform, *not how*
  – API targets compiler, not hardware primitives
  – API independent of underlying hardware

• Goals: intuitive programming models and application portability
  – from other little-endian environments
    • consistently little-endian API and data layout
  – from big-endian environments (Power BE)
    • simplify porting and sharing of libraries between LE and BE environments
    • exploit large body of numeric middleware developed for Power
The “True Little-Endian” Vector Model  (Default LE Vector API)

- OpenPOWER Little-Endian Model
  - Focus on programmability – consistent little-endian view
  - Focus on ease of sharing code with other little-endian ecosystems
The “Big-on-Little-Endian” Vector Model  (Optional BE Portability Model)

- “Big-on-Little-Endian” Model ➔ Optional Model for Porting of BE Libraries
  - Focus on porting of Big-Endian code with Big-Endian register layout
  - Focus on ease of sharing code between LE and AIX / BE Linux

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<table>
<thead>
<tr>
<th>Byte Index</th>
<th>0</th>
<th>...</th>
<th>15</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Memory address</th>
<th>E[0]</th>
<th>E[1]</th>
</tr>
</thead>
</table>

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OpenPOWER Little-Endian API Implementation

• Vector API model selected by command line switch
  – Native (default) API is to “True Little Endian”
  – Compiler command line to select “Big-on-Little” (GCC,XL)

• Compiler-based mapping of vector API to hardware primitives
  – True LE ➔ hardware instructions use big-endian register numbering
  – Big-on-Little ➔ bridge BE/LE data layout on memory accesses
    • Power ISA provides support for transparent data adjustment

• Both models translated to common intermediate format
  – Compiler optimizes vector computations
OpenPOWER available now

- Collaborative innovation already changing industry
  - Major data center stakeholders joining OpenPOWER

- Redefined software stack: Firmware, Hypervisors, OS, Applications
  - little-endian data model for simplified application porting
  - Linux distros available now ➔ 40000 packages ported

- New OpenPOWER environment enables
  - ease-of-use and out-of-box performance
  - exploitation of new Power8 hardware features
Thank you!
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