NMI: A New Memory Interface to Enable Innovation

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Introduction – Problems Faced in Memory Systems
Memory subsystem impacts performance, energy, and cost

- Point-to-point networks of NMI Nodes (any combination of ports, switches, memories and processing elements). Master nodes for local control and subnets for massive scalability
- Abstracted, flexible timing interface supporting diverse technologies
- HSA-compatible virtual memory, cache coherency, task dispatch
- Optional feature set profiles to scale cost, area and complexity from embedded to supercomputer systems
- Scalable ECC tunable for application, including memory RAID
- Multiple physical to device mappings for custom interleaving
- Abstracted power modes for global management with mixed devices

NMI Protocol Layers
(1) Physical Layer: Flexible (electrical/optical/other), under development
(2) Link Layer: Packetized, reliable, scalable header overheads, virtual channels for deadlock avoidance, and low latency
(3) Transaction Layer: Classes of optional functionality as follows;

<table>
<thead>
<tr>
<th>#</th>
<th>Class</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Foundation &amp; Computation</td>
<td>Non-coherent R/W, capability query, logical memory region management, task dispatch</td>
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<tr>
<td>1</td>
<td>Atomics</td>
<td>Atomic operations</td>
</tr>
<tr>
<td>2</td>
<td>Virtual Memory</td>
<td>Address translation, TLB invalidation</td>
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<td>3</td>
<td>Coherence</td>
<td>Cache coherence</td>
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<tr>
<td>4</td>
<td>Fixed-Function Units</td>
<td>Gather/Scatter, reduction, initialization, etc.</td>
</tr>
<tr>
<td>5</td>
<td>Advanced ECC</td>
<td>Memory RAID support</td>
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<tr>
<td>6</td>
<td>Persistent Memory</td>
<td>Fence, flush, freeing address ranges</td>
</tr>
<tr>
<td>7-12</td>
<td>&lt;reserved&gt;</td>
<td>Reserved for future standard features</td>
</tr>
<tr>
<td>13-15</td>
<td>&lt;vendor-defined&gt;</td>
<td>Vendor-defined</td>
</tr>
</tbody>
</table>

NMI Power Management
High-level (abstract) power mode and low-level (direct) power mode

Other challenges: Interface compatibility between different memory types, workload adaptation to different memory types, and reliability due to process technology scaling, multi-level cells, and capacity increase

Novel Features
- Addressing, region freeing Atomic TLB R/W, to different memory types, and GPGPU invalidation

Various memory technologies, such as the heterogeneous system architecture (HSA) allow Host and PIM processors to share memory and work

Abstacted memory interfaces are becoming more important due to the emergence of diverse non-volatile memory technologies

Heterogeneous memory technologies can be used together to reduce cost while providing performance, capacity, and non-volatility

Hardware vs Managed NMI Networks
Unmanaged example: Small-scale, low-latency, low-overhead
Managed example: Scalable to many nodes, divided to subnets, each managed by a Master node

Logical Memory Regions
Logical division of physical memory address space into non-overlapping, contiguous regions
Each memory region has its own:
- Physical-to-device address mapping
- Size and address range
- Multi-level cell configuration

Conclusions
NMI is an abstracted, unified memory interface to support future scale-out memory capacity, processing-in-memory, I/O devices, emerging non-volatile memories, cache coherency shared virtual memory

A New Memory Interface To Enable Innovation**
- Existing memory interface protocols present a barrier to overcoming key problems and providing scalable, compatible ‘smart’ memory components from multiple vendors, from cellphones to supercomputers
- This work is in progress in overcoming these key problems