Architecture for Carbon Nanotube Based Memory (NRAM)
Agenda

• Carbon nanotube basics
• Making & breaking connections
• Resistive measurements
• Write endurance, Timing, & Temperature
• When DRAM fades away
• The universe of Storage Class Memories
• NRAM: Memory Class Storage
• Standard modules using NRAM
• Industry readiness for persistent memory
Disclaimer

• Nantero is a technology development and intellectual property licensing company
• This presentation covers the technology we develop and license
• Details shown apply to a specific reference design
• Specific product details and introduction dates relate to availability of the technology
• Customers & partners control actual product details and dates
• We’d be thrilled to license to YOU, too 😊
Van der Waals effect keeps CNTs apart or together

Data retention >300 years @ 300°C (more likely >1000 years)

Stochastic array of many nanotubes per each cell
No Dielectric $\rightarrow$ No Known Failure Mechanism

- CNTs switch in a void
- No dielectric
- Wear-out has not been observed
- Unlimited write endurance expected
Resistance Measurements, 0 and 1

Greater than 10X difference between ‘0’ and ‘1’...
No calibration required across the wafer
Smooth SET curve: MLC has been tested as well
Pulse Width Timing, Reset $\rightarrow$ 0, Set $\rightarrow$ 1

Consistent operation from 40 ns down to 5 ns read/write per cell

And very repeatable
No Apparent Temperature Sensitivity

Similar set & reset curves at any temperature
CNT operation and retention seen at 300°C, > 300 years
Limited by underlying silicon circuit reliability
NRAM Capacity Scaling

- Add layers of CNTs
- Process agnostic... Can be built on top of memory or logic processes
- Multi-level cell as a function of pulse
- Example: 4Gb/layer w/ 28nm logic
- Process scaling is a function of #CNTs per bit... well understood < 5nm

Note: Reference design detail; may vary by customer
DDR NRAM Scalability

- 8 Gb
  - 28 nm logic
  - 2 layers CNT
  - 8-die stacks

- 16 Gb
  - 28 nm logic
  - 4 layers CNT
  - New process
  - ~100 mm²

- 64 Gb
  - 14 nm
  - 4 layers CNT
  - New process
  - Add layers

- 128 Gb
  - 14 nm
  - 8 layers CNT
  - New process
  - Add layers

- 256 Gb
  - 7 nm
  - 8 layers CNT
  - New process
  - Add layers

- 512 Gb
  - 7 nm
  - 8 layers CNT
  - New process
  - Add layers

- 1024 Gb
  - 7 nm
  - 8 layers CNT
  - New process
  - Add layers

Note: Reference design detail; may vary by customer
NRAM is a “Memory Class Storage”

- Hard Disk
- SSD
- NVMe
- Wasteland
- DDR
- DRAM

- Flash

- 3D NOR
- Phase Change
- 3D Xpoint
- Resistive
- Magnetic

- > DRAM performance
- = DRAM endurance
- > DRAM capacity
- < DRAM price

- Painfully slow
- Lotsa cheap bits
- Low endurance

- Moderate speed
- Moderate endurance
- Capacity range

- DDR
- NRAM
Note: Reference design detail; may vary by customer
Crosspoint Tiles

Tile = 64 x 256 x 4

Latching sense amplification

Select Decode Logic

Note: Reference design detail; may vary by customer
Timing Impact of On-the-fly ECC

<table>
<thead>
<tr>
<th></th>
<th>DDR4 SDRAM (ns)</th>
<th>DDR4 NRAM (ns)</th>
<th>DDR5 SDRAM (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Row cycle</td>
<td>47.00</td>
<td>46.25</td>
<td>50.18</td>
</tr>
<tr>
<td>Access time</td>
<td>17.14</td>
<td>13.50</td>
<td>18.18</td>
</tr>
<tr>
<td>Row to column</td>
<td>15.00</td>
<td>23.00</td>
<td>18.18</td>
</tr>
<tr>
<td>Precharge</td>
<td>15.00</td>
<td>14.25</td>
<td>18.18</td>
</tr>
<tr>
<td>Write recovery</td>
<td>15.00</td>
<td>23.00</td>
<td>45.00</td>
</tr>
<tr>
<td>Activate to precharge</td>
<td>32.00</td>
<td>32.00</td>
<td>32.00</td>
</tr>
<tr>
<td>Refresh</td>
<td>350.00</td>
<td>0</td>
<td>350.00</td>
</tr>
</tbody>
</table>

Note: Reference design detail; may vary by customer
Bus Efficiency Comparison at Same Frequency

- DDR4/DDR5
  - Base throughput
  - Elimination of refresh
  - Elimination of ACTIVATE restrictions
  - Elimination of bank group restrictions
  - Elimination of power states

- NRAM

~15%
128 GB NRAM LRDIMM or RDIMM

Host reads SPD, configures memory interface per settings

Fully Deterministic DDR Memory interface
For Comparison, Industry NVDIMM-N

Flash backup for DRAM

External energy source & regulation

Half DRAM
Half Flash

Power Supply

NVC

DRAM

DB

FLASH

DB

DB

Power Supply

External energy source & regulation

NVC

DRAM

DB

DRAM

DB

DB

DB

DB

DB

Flash backup for DRAM

External energy source & regulation

NVC

DRAM

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Flash backup for DRAM

External energy source & regulation

NVC

DRAM

DB

DB

DB

DB

DB
Non-deterministic protocol needed because other NVMs have wear out and need leveling.
Power Fail Comparison

**NVDIMM-N, -P**
- Complete burst in process
- Switch power to battery
- Save all pending operations
- Copy DRAM to NVM

**A minute or more...**
- Check save status
- Copy NVM to DRAM
- Run

**NRAM Module**
- Complete burst in process
- Run
Software Increasingly Persistence Aware

Windows, Linux exploit persistent memory
Summary

• Electrostatic effects set & reset each bit
• Resistance delta of 10X allows reliable sensing
• Dielectric-free cell shows no wear-out
• DDR4 NRAM includes a DRAM-compatible front end
• Defines a new category “Memory Class Storage”
• NRAM per die capacity scales far beyond DRAM
• Fully deterministic timing better than a DRAM
• On-the-fly ECC incorporated for server class reliability
• Module level NRAM products are plug and play compatible
• Industry is ready for persistent main memory
Thank you for your time

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