**Ferric**

On-chip Magnetic Thin-Film Inductors Enable Integrated Power Management

- **Key Features**
  - Multi-phase Interleaved Power Train with Thin-Film Magnetic Inductors
  - High switching frequency >160MHz
  - High bandwidth regulation >50MHz
  - Output Low Dropout Linear Regulator
  - Gang operation
  - Auto Phase Shedding, Dynamic Voltage Scaling (DVS)
  - 1MHz PMBus-Compliant Serial Interface

- **Benefits**
  - Power Savings of 10-50%
  - Reduction of board area >50%
  - Reduction in BOM >25%

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**Integrated Power Management improves power integrity, energy efficiency, and data bandwidth**

Integrated Voltage Regulators significantly alleviate the data + power bottleneck while reducing PDN impedance. Reduced current levels in upstream PDN save 12R losses while reduced PDN impedance at the load allows for reduced supply voltage margins, combined with improved power management to save >25% total power.

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**Design IP for Monolithic Voltage Regulator**

**Ferric IVR IP in Customer SoC**
- Array of Inductors placed above SOC logic
  - >10A/mm² effective current density
- Power distribution across die on top metal under inductor
  - ~3x reduction in input and ground supply current
- Power FETs placed in regular array in FEOL with inductors
  - ~70A/mm² FEOL current density

**Customer Requirements:**
- CMOS Process
- Input & Output Voltage
- Load-CURRENT & Phase Count
- Supply Count
- Feedback Compensation & Decoupling
- Feature Set

**Ferric Deliverables:**
- Model (Verilog, Verilog-A, SPICE)
- Layout (GDSII)
- Netlist (CDL)
- Abstract (LEF)
- Timing (LIB)
- Datasheet & Assembly Guide

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**Microscope Image of Ferric Inductors**

**Illustration of Ferric inductors in CMOS IC**

**Microscope Image of Ferric single-chip power converter**

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**Ferric Package Voltage Regulators (PVR) for HPC**

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**Conventional PDN**

- **PDN with PVR**
  - Board Voltage Regulator
  - Processor

**Conventional VRM on board SoC on substrate**

- PDN with Pre-Reg
  - 1.5V Pre-Regulator
  - Processor

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**Efficiency, Vin: 1.6V, Fsw: 180.0MHz Temp: 27.0°C**

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<th>Efficiency (%)</th>
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**Vin: 2.0V, Fsw: 180 MHz, Temp: 85°C**

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**Film Inductors**

Networks which are slow to inducing power distribution by on Amperes and are restricted PVR9

**PVR8**

**PVR10**

**PVR11**

**PVR12**

**PVR13**

**PVR14**

**PVR15**

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**Illustration of MVR floorplan – Inductors & Bumps**

**Illustration of MVR floorplan – Power FETs in FEOL**

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