Lakefield: Hybrid cores in 3D Package

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Lakefield: Design goals

• High level goal:
  • Enable new class of compute devices in Mobility form factor (converged Mobility)
  • Best in class Compute performance in lower TDP
  • Always on, always connected, very low standby Power

• What this meant to Compute SOC
  • Migrate to latest Process technology/ Intel 10nm
  • Significant Gen over Gen improvements:
    • ~1/10th Standby Power
    • ~50% GFX improvement
    • ~40% Core area reduction
    • ~40% Z reduction

• How do you achieve this in 1 Generation?
  • Birth of Lakefield!
Lakefield Big picture: Small Form Factor Devices

PoP Package: 12.00 x 12.00 mm

12.0 mm Package

1.00 mm Post SMT
Lakefield vs Prev gen vs Comp

LKF Dual Display AEP
- 30 x 123
- LTE MODEM

LKF Clamshell AEP
- 30 x 171
- LTE MODEM

Gen-1 AEP
- 30 x 232
- LTE MODEM

COMP motherboard
- 43 x 286

Key enabling vectors

<table>
<thead>
<tr>
<th>Category</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SoC</td>
<td>Hybrid CPU architecture</td>
</tr>
<tr>
<td>Package</td>
<td>3D Foveros packaging</td>
</tr>
<tr>
<td>PCB</td>
<td>Compact 30x123mm LKF motherboard design</td>
</tr>
<tr>
<td></td>
<td>0.6mm, 10L, ALV, complete single sided</td>
</tr>
<tr>
<td>EC</td>
<td>EC-lite architecture</td>
</tr>
<tr>
<td>Boot</td>
<td>SPI-less boot from UFS</td>
</tr>
<tr>
<td>Form factors</td>
<td>Dual/foldable displays; thin clamshells</td>
</tr>
</tbody>
</table>
## Core area attributes

<table>
<thead>
<tr>
<th></th>
<th>Y SKU Gen-1</th>
<th>Y SKU</th>
<th>LKF</th>
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<tbody>
<tr>
<td>Core area attributes</td>
<td>mm²</td>
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<tr>
<td>Core</td>
<td>1x</td>
<td>0.9x</td>
<td>0.4x</td>
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<tr>
<td>Package</td>
<td>20.5x16.5</td>
<td>26.5x18.5</td>
<td>12x12</td>
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<tr>
<td>Memory</td>
<td>LP3 11x11.5</td>
<td>LP4-4x 12.5x12.5</td>
<td>LP4-4x POP</td>
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<tr>
<td>Power Delivery</td>
<td>Discrete VR</td>
<td>FIVR/ Discrete VR</td>
<td>PMIC</td>
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</table>
LAKFIELED ARCH: Hybrid cores + 3D Die stacking

- Latest Display core: 4 pipes, 5k60 or 4k120
- Latest GFX core: Gen 11 64EUs
- Latest Media core: 4k60/8k30
- Latest IPU 5.5: up to 16MP, x6 connected cameras
- Compute die: 10nm
- Base die: P1222

New Hybrid IA cores
1x SNC + 4x TNT

SNC Core-BIG
TNT Core-ATOM
TNT Core-ATOM
TNT Core-ATOM
TNT Core-ATOM

Gen 11 GFX Core
Gen 11 Media
Gen 11.5 Display Core
IPU 5.5 Img Core
DDRIO/LP4x-4267

Audio
USB2/3
UFS3
PCIE Gen3
ISH

I3C
SDIO
CSE
TC SS
SPI/I2C
No single transistor node is optimal across all design points!
INTEL process DEVELOPMENT MODEL w/ Foveros

Manufacturing

Optimized for Compute

1274(10nm)

“FOVEROS”

P1222

Development

1276(7nm)

1274.FV

Path finding

1278

1276.FV

Optimized X/Y, board area
Mix and Match of IP and process nodes.
Highest Performance & Lowest Leakage
Allows IPs to be developed independently, faster time to market

Ultra-Mobile form factor (12x12x1 mm package)
~2.x mW Standby Battery Life
Leadership CPU Performance

Lakefield implementation
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PC in Mobile form factor – 12x12
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Chipset, power Delivery, Low power logic - P1222 Base
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High Bandwidth, ultra low power connectivity between Dies
Scalable TSV for power delivery
High Yielding process for Die 2 Wafer Attach, Thermal solution to enable 3D stacking
lakefield foveros

10 nm compute process for Cores and Graphics
lakefield foveros

DRAM integration in 1 mm Z height
Advantages of Hybrid compute

- Big-Bigger Compute combination, ideal for mobility compute use case
- Heavy compute, bursty workload on SNC core
- Light compute workload on ATOM/Tremont, w/o compromising on performance
- Low power scenarios that are key to Battery life run on Tremont cores
SNC Bigger Core delivers
- Single Thread Performance and Efficiency at burst

TNT Efficient Atom cores deliver
- MT perf and core count/area efficiency
- Power Efficiency with realistic workloads
- Battery Life (HoBL)

For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.
IA hybrid architecture

- Dynamic feedback to the OS/SW on Hybrid Core PnP capabilities
- Performance/responsiveness threads scheduled on SNC core
- Background and threads scheduled on TNT cores
- All cores execute threaded/concurrent applications
Gen over gen Connected Standby improvements

Lake Field Connected Stand Power

<table>
<thead>
<tr>
<th></th>
<th>6th Gen Core</th>
<th>8th Gen Core</th>
<th>Lakefield</th>
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<tbody>
<tr>
<td>1.0X</td>
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Architecture, Process & Design Optimizations
1. IP partitioning between Compute & Base
2. Vnn Removal, LDO removal and low leakage power gating in base die
3. USB and DDR Phy improvement
4. Very Low leakage transistor usage
5. Logic, Memory, and Clock IP Power scaling

For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.
Lakefield graphics improvements

Lakefield GFX performance @7W

- 9th gen GFX: 1.0X
- Manhattan: 1.53X
- 3DMark11: 1.64X
Lakefield Summary

• LKF introduces first in the industry, a product with 3D stacking, and IA hybrid computing
• First PC Compute SOC with dimensions of 12 x 12 x 1 mm, and Standby power of 2.x mW
• LKF designed for lower power, to enable new thin/ form-factors, 2 in 1’s, dual-display devices
• LKF architecture has significant improvements over previous generation with ~0.1x S0iX3, ~0.5x PCB Core area and ~1.5x GFX performance
• Silicon is in final phase of production readiness targeting end of Q4’19
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