June 26, 1989 — Kresge Auditorium, Stanford University

Monday

8:45–9:00  Welcome and Opening Remarks
Robert G. Stewart, General Chair

9:00–10:45  New SPARC CPUs
Chair: Dave Ditzel, Sun Microsystems

- Cypress SPARC Program Overview
  Raju Vegesna, Ross Technology
- ECL SPARC Chip Set
  Anant Agrawal, Sun Microsystems/Bipolar Integrated Technology
- The Architecture of the P1—A 250 MHz SPARC in GaAs
  Pete Wilson, Prisma

10:45–11:00  Coffee Break

11:00–12:30  RISC CPU Updates
Chair: Forest Baskett, Silicon Graphics

- Fujitsu SPARC Chip Set Update
  Rolando Carreras, Fujitsu Microelectronics, Inc.
- L64815 MCT Overview
  Douglas Grundman, LSI Logic
- 88K Family Update
  Mitch Alsup, Motorola
- MIPS RISC Architecture
  John Mashey, MIPS Computer
- Clipper Update
  Harlan McGhan, Intergraph

12:30–1:30  Lunch & Walkabout Stanford Campus

1:30–2:15  Invited Speaker: Professor W. Kahan, UC Berkeley
“Bumps on the Path to Floating Point Progress”

2:30–3:30  New Processor Architectures
Chair: Jack Grimes, MASS Microsystems

- Intel i860 Million Transistor 64-bit Microprocessor
  Les Kohn, Intel Corporation

3:30–4:00  Soda Break

4:00–5:30  Floating Point Processors
Chair: Dave Goldberg, Xerox Corporation

- ABACUS 3170/3171 Single Chip FP Coprocessor for SPARC
  Allen Samuels & Mark Birman, Weitek
- The TMS390C602 SPARC FPU
  Merrick Darley, Texas Instruments
- L64814: LSI Logic’s SPARC Floating Point Coprocessor
  Peng Ang, LSI Logic
- The MIPS R3010 FPU
  Earl Kilian, MIPS Computer

6:00–8:30  Reception In Bowman Oak Grove near Tresidder Union

Organizing Committee for the HOT Chips Symposium:
Dr. Robert G. Stewart, General Chair, Stewart Research Enterprises

Hasan Alkhatib, Registrar  Martin Freeman, Treasurer
Santa Clara University  Philips Research Lab
Dave Ditzel, Program  Jack Grimes, Program
Sun Microsystems  MASS Microsystems

Robert Hatch
Kaiser Electronics
Glen Langdon, TC Chair
University of California, SC
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8:45–10:30 New CISC CPUs
Chair: Mark Horowitz, Stanford University
- Motorola 68040 Introduction
  Motorola Semiconductor
- Intel's i486 Processor Architecture
  John Crawford, Intel Corporation
- Pipeline Control for a Single-Cycle VLSI Implementation of a
  Complex Instruction Set Computer
  David R. Stiles & Harold L. McFarland, NexGen

10:30–10:45 Coffee Break

10:45–12:30 Embedded CPUs
Chair: John Wakerly, Stanford University
- Intel's 860 RISC Family
  Steve McGeady, Intel Corporation
- Meeting the Embedded Challenge: National's NS32GX32,
  The New Generation
  Jonathan Levy, National Semiconductor
- AMD 29000 Update
  Brett Stewart, AMD

12:30–1:30 Lunch & Walkabout Stanford Campus

1:30–3:00 Graphics Coprocessors
Chair: Jack Grimes, MASS Microsystems
- The TMS34020 Graphics System Processor and the TMS34082
  Floating Point Co-Processor
  Mike Asal, Texas Instruments
- Sun GX Graphics Workstations, The Standard for Graphics
  Performance from the Desktop to Powerful Desktop Systems
  Curtis Priem, Sun Microsystems

3:00–3:30 Soda Break

3:30–5:00 Panel Session: Compiler Issues with HOT Chips
Chair: John Mashey, MIPS Computer
- Tom Pennello, MetaWare
- Steve Johnson, Ardent Computer
- Steve Glanville, Silicon Valley Software Trio
- Michael Tiemann, Stanford University

5:00 Adjourn

Program Committee for the HOT Chips Symposium:
Dave Ditzel and Jack Grimes, Co-Chairmen

Forest Baskett
Silicon Graphics, Inc.

Mark Horowitz
Stanford University

John Wakerly
Stanford University

Dave Goldberg
Xerox PARC

John Mashey
MIPS Computer Systems