COMPILING FOR HOT CHIPS

Stephen C. Johnson
Ardent Computer
880 W. Maude
Sunnyvale, CA 94086

TRENDS

DATA MOVEMENT > COMPUTATION

Register Allocation
Cache Management
Dependency Analysis

PARALLELISM

Multiprocessor systems
Independent Coprocessors
Vector and vector-like instructions
Long Instruction Word machines
IS RISC JUST GOOD SYSTEM DESIGN???

CPU's AND COMPILERS MISMATCHED

... at least, historically

But not with RISC

Berkeley RISC :: PCC
Stanford RISC :: Optimizing Pascal
801 :: PL/8

... at least for a while

Sparc :: ??
88000 :: ??
i860 :: ??

CRISIS -- COMPILERS LAG HARDWARE

repeat

{

Compiler writers work on last generation
Chip designers design next generation
THUS: next chips hard to compile for

} until ( we wise up )

SIMILAR PROBLEM WITH OS

BIG PROBLEM WITH MULTIPROCESSING

It's not possible to do a good job treating
multiprocessing as an afterthought!
WHAT TRENDS IN COMPILER TECHNOLOGY?

PARALLEL COMPILATION

Mathematically, looks like chip layout
Laying out operations in 2D
For VLSI, x and y
For parallel, CPUs and time
Silicon compiler techniques apply:
  Simulated Annealing
  Kernighan-Lin-Fiduccia
  ...

SUCCESS WILL COME TO GOOD SYSTEMS

  ... not just good chips