Outline

1. RC6280 System Overview
2. Technology
3. R6000 Chip Set
4. Cache Organization
5. Performance
6. Future Directions
Design Goals

- Fastest complete system for $150,000
- Single-board processor
- Highly integrated VLSI chip set
- I/O and memory commensurate with processor
- Compatible with user-level R2000 instruction set

RC6280 Performance / Expansibility

- 50 VUPS (VAX Units of Performance) @ 60 MHz
- 9 double precision Linpack megaflops (compiled)
- 240 megabytes/sec (peak) backplane bandwidth
- one to six VME busses
- 1 gigabyte main memory with 4 megabit chips
RC6280 Architectural Features

- Two level cache
- 36-bit physical address
- R2000 instruction set with enhancements
  - Load/Store double floating-point
  - Synchronization (load-locked, store-conditional)

RC6280 System Block Diagram
Technology Overview

- ECL VLSI using standard cell design methodology
- Small, fast ECL gate arrays for VLSI to cache interconnect
- 8 ns 4Kx4 and 16Kx4 primary cache RAMs (ECL, BiCMOS)
- 15 ns 64Kx1 secondary cache RAMs (BiCMOS)

- All components designed for air-cooling at 400 LFM (45° C rise)
- VLSI devices packaged in 259-pin ceramic PGAs
- 100K temperature compensated signal levels
- Buried termination resistors to reduce stubs at PGAs
R6000 Chip Set

- four VLSI chips -- CPU, FPC, FMPY, Bus
- tightly coupled CPU/FPC interface
- system bus completely defined by Bus chip
- on-chip address translation and cache control

R6000 Chip Set Physical Parameters

<table>
<thead>
<tr>
<th></th>
<th>R6000 CPU</th>
<th>R6010 FPC</th>
<th>R6020 Bus</th>
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<tbody>
<tr>
<td>die size (mm)</td>
<td>9.9x10.1</td>
<td>9.9x9.6</td>
<td>9.4x9.6</td>
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<tr>
<td>power</td>
<td>23W</td>
<td>20W</td>
<td>20W</td>
</tr>
<tr>
<td>transistor count</td>
<td>89K</td>
<td>88K</td>
<td>91K</td>
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<tr>
<td>resistor count</td>
<td>54K</td>
<td>54K</td>
<td>66K</td>
</tr>
<tr>
<td>number of cells</td>
<td>4468</td>
<td>4238</td>
<td>4002</td>
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<tr>
<td>signal pins</td>
<td>184</td>
<td>173</td>
<td>155</td>
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<tr>
<td>package pins</td>
<td>259</td>
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</table>
Cache Organization

- two-level cache (64K I, 16K D, 512K Secondary)
- separate primary caches, combined secondary cache
- virtually indexed primary, physically indexed secondary
- virtual tags on both caches
- on-chip TLB slice, in-cache full TLB
- entire design requires only six banks of RAM

Processor Block Diagram
Primary Caches

- Primary instruction cache
  - direct mapped
  - 8-word line size
  - refill -- 10 cycles and restart

- Primary data cache
  - write-through
  - 2-word line size
  - refill -- 1 cycle and restart

- Virtual addresses and virtual tags (including PID)
- Shared tag -- pretest mechanism

Secondary Cache

- 512 Kbytes - 2 Megabytes
- two-way set associative
- physical addresses, virtual tags (including PID)
- 32-word line size
- write-back
- two cycle access to each side
- ping-pong for block transfers at one word per cycle
- refill -- 65 to 80 cycles
Secondary Cache Lines

<table>
<thead>
<tr>
<th>Word 0</th>
<th>Bank 0</th>
<th>Set 0</th>
<th>Set 0</th>
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<tbody>
<tr>
<td>Word 1</td>
<td></td>
<td>Set 1</td>
<td>Set 0</td>
</tr>
<tr>
<td>Word 2</td>
<td></td>
<td>Set 0</td>
<td>Set 1</td>
</tr>
<tr>
<td>Word 3</td>
<td></td>
<td>Set 1</td>
<td>Set 0</td>
</tr>
<tr>
<td>Word 4</td>
<td></td>
<td>Set 0</td>
<td>Set 1</td>
</tr>
<tr>
<td>Word 5</td>
<td></td>
<td>Set 1</td>
<td>Set 0</td>
</tr>
<tr>
<td>Word 31</td>
<td></td>
<td>Set 1</td>
<td>Set 0</td>
</tr>
</tbody>
</table>

Address Translation

- no translation to primary caches
- physical index to secondary cache is simpler for OS
- 6-bit wide TLB slices in CPU-- separate instruction and data
- TLB and physical tags held in reserved portion of secondary cache
- full-width TLB read only after secondary cache miss
Virtual PN

Virtual tag

data

tlb slice

cmp

hit/miss

address

cache

PID | Virtual PN | offset
---|------------|---

PID virtual page number offset

Virtual tag + Index

Primary Cache

PID virtual tag data

compare

hit/miss

physical index

Secondary Cache

PID virtual tag data

compare

hit/miss

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Secondary Cache Organization

Secondary Cache Miss Sequence

- detect virtual miss
- read TLB entry
- check for TLB miss
- check for TLB slice miss
- read physical tags -- compare with TLB entry to detect physical hit
RC6280 Performance:
SPEC Rating - 42.5 SPECmarks
Future Directions

- Faster transistors
- Smaller metal and via pitches
- More layers of metal
- Lower capacitance
- Multiple voltages (GND, -5, -2)
- Higher power

<table>
<thead>
<tr>
<th>Single chip CPU/FPU</th>
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<tbody>
<tr>
<td>Wider data paths to cache</td>
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<tr>
<td>Highly integrated caches</td>
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<tr>
<td>Deeper pipeline</td>
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<tr>
<td>Multiple instruction issue</td>
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