**Introducing a Revolutionary 3 Dimensional Package Type**

**THE SLCC**

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<table>
<thead>
<tr>
<th>Dimension</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIGHEST STACK</td>
<td>Multi-chip Module using Stackable Leadless Chip Carriers (SLCC)</td>
<td></td>
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<tr>
<td>DSMCM</td>
<td>Double sided multi-chip modules</td>
<td></td>
</tr>
<tr>
<td>HYBRID</td>
<td>Several die in 1 package</td>
<td></td>
</tr>
<tr>
<td>HIGHER QFP</td>
<td>Quad flatpack</td>
<td></td>
</tr>
<tr>
<td>PGA</td>
<td>Pin grid array</td>
<td></td>
</tr>
<tr>
<td>LCC</td>
<td>Leadless chip carrier</td>
<td></td>
</tr>
<tr>
<td>CIRCUIT PLCC</td>
<td>Plastic leadless chip carrier</td>
<td></td>
</tr>
<tr>
<td>DENSITY SOJ</td>
<td>Small Outline Package</td>
<td></td>
</tr>
<tr>
<td>SOIC</td>
<td>Small Outline I.C.</td>
<td></td>
</tr>
<tr>
<td>FP</td>
<td>Flatpack</td>
<td></td>
</tr>
<tr>
<td>LOWER DIP</td>
<td>Dual in line package</td>
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Multiple connections of the conventional type packages are done in a 2-dimensional plane. Multiple connections of the Stackable Leadless Chip Carrier are done in 3 Dimensions, therefore a higher circuit density can be accomplished.

**FEATURES OF SLCC’s**

- Surface Mount technology
- Stackable ceramic leadless chip carrier
- Hermetically sealed
- Pinout internally and/or externally configurable
- Operates over full military temperature range
- Typically Single I.C. (Can Accept Multiple)
- Can easily mirror pinouts
- Small size
ANY NUMBER OF PACKAGES CAN BE STACKED TO FORM A LOGICAL CIRCUIT SUBSYSTEM.
DENSE-STACK FEATURES

- Able to Parametrically Test Components at Temperature Before Assembling Stack.
- Able to Environmentally Screen and Burn-In Components Before Assembling Stack.
- Able to Rework and Replace Bad Components After Stack has been Assembled.
- Able to Visually Inspect All Components After Assembling Stack (No Hidden/Buried Solder Connections).
- Able to Clean and Remove Flux Residue Because of Standoff Between Stacked Components.
- Better Electrical Performance Due to Extremely Short/Low Resistance Interconnects Between Components in Stack.

Circuit Board Features
(Using Dense-Stack)

- Able to Upgrade or Revise Circuit Without Changing PWB Design.
- Increases Memory Density
  - Reduced Number of Layers
  - Reduced Number of Vias
  - Reduced Trace Lengths
  - Reduced Number of PWB's
- Operates over Full Military Temperature Range
COMPARISON OF PCB SPACE REQUIRED FOR A 16 MEGABYTE SRAM SYSTEM FOR DIFFERENT PACKAGE TYPES.

<table>
<thead>
<tr>
<th>PACKAGE TYPE</th>
<th>DIP</th>
<th>SOIC</th>
<th>SOI</th>
<th>LCC</th>
<th>2-SLCC</th>
<th>4-SLCC</th>
<th>8-SLCC</th>
<th>16-SLCC</th>
<th>32-SLCC</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB AREA</td>
<td>0</td>
<td>25</td>
<td>50</td>
<td>75</td>
<td>100</td>
<td>75</td>
<td>50</td>
<td>25</td>
<td>0</td>
</tr>
</tbody>
</table>

COMPARISON OF PCB SPACE REQUIRED FOR A 16 MEGABYTE SRAM SYSTEM FOR DIFFERENT PACKAGE TYPES.

GENERIC SLCC APPLICATION

THICK FILM RECONFIGURATION SUBSTRATE

RECONFIGURATION SUBSTRATE ALLOWS ANY DIE CONFIGURATION OF N OR LESS BOND PADS TO BE CONFIGURED AT WILL TO THE LCC PINS.
AT THE STACK LEVEL

THE FEATURES NEEDED FOR A STACKABLE APPLICATION ARE CIRCUITS WITH SIMILAR DEVICES WITH HIGH NUMBER OF COMMON I/O AND PARALLELED CONTROL SIGNALS. EXAMPLES: MEMORY, MULTIPLEXERS, BUS INTERFACE, MULTIPROCESSORS.

SINGLE - INSTRUCTION - MULTIPLE - DATA
MULTIPROCESSOR
INTERCONNECTION SYSTEM

FEATURES:

- 1.4" X 2.0" X 0.5" OUTER DIMENSIONS
- 160 PINS
- USES 48 - 157's (QUAD 2-INPUT MULTIPLEXERS)
- 8-BIT DATA PATH
- INDIVIDUAL SWITCHING BLOCK CONTROL PINS
- SAVE 256 PINS