SILICON MULTIChip MODULES

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nCHIP, Inc.

AGENDA

LIMITATIONS OF SINGLE CHIP PACKAGING SOLUTIONS

nCHIP’S MCM (MULTIChip MODULE) SOLUTION

AN MCM APPLICATION (ROSS TECHNOLOGY)
INCREASING CHIP I/O IS A MAJOR COST CONSIDERATION

- High performance packages cost 5-10¢/pin
  - A 400 pin IC package can cost more than $40

- More expensive PCBs (printed circuit boards) are required:
  - PCB interconnect density requirements increase as:
    Interconnect density \( \sim \) (# of chip terminals/chip pitch)
  - PCB cost increases rapidly with increasing interconnect density

CAPACITANCE LIMITATIONS

- High performance, impedance controlled packages have high pin capacitance (5 - 8 pF/pin)

- PCB interconnect technology contributes
  - 3 - 4 pF/in
  - \( \sim \) 1 pF/plated through-hole

- "Capacitive" delay of interconnect in CMOS systems (PCB) is often more than 4 ns
WHEN DOES LEAD INDUCTANCE BECOME A PROBLEM?

The voltage drop on a package lead is:

\[ \Delta V = -L_{lead} \frac{di}{dt} = -L_{lead} \left( \frac{V_0}{Z_0} \right) t_{rise} \]

If you want \( \Delta V/V_0 = 0.1 \) and \( Z_0 = 50 \Omega \), then:

<table>
<thead>
<tr>
<th>( t_{rise} ) (ns)</th>
<th>( L_{lead} ) (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>5.0</td>
</tr>
<tr>
<td>0.5</td>
<td>2.5</td>
</tr>
<tr>
<td>0.2</td>
<td>1.0</td>
</tr>
</tbody>
</table>

If you have \( N \) lines switching at once: \( \Delta V = -N L_{power} \frac{di}{dt} \)

For \( N=40 \):

<table>
<thead>
<tr>
<th>( t_{rise} ) (ns)</th>
<th>( L_{power} ) (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>0.12</td>
</tr>
<tr>
<td>0.5</td>
<td>0.06</td>
</tr>
<tr>
<td>0.2</td>
<td>0.025</td>
</tr>
</tbody>
</table>

LEAD INDUCTANCE FOR SINGLE-CHIP MODULES (180 I/O)*

<table>
<thead>
<tr>
<th>Wirebonded</th>
<th>TAB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin Grid Array</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Substrate Size (mm²)</th>
<th>Wirebonded</th>
<th>TAB</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>36</td>
<td>30</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Lead Inductance (nH)</th>
<th>Wirebonded</th>
<th>TAB</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Min.)</td>
<td>7.0</td>
<td>8.5</td>
</tr>
<tr>
<td>(Max.)</td>
<td>24</td>
<td>12.5</td>
</tr>
</tbody>
</table>

Package lead inductance poses substantial performance limitations

SINGLE-CHIP PACKAGING LIMITATIONS

- Single-chip packaging solutions have a major effect on system performance and cost
  - Capacitance, inductance, and long interconnect distances substantially reduce system performance
  - High pin count ICs require expensive packages and PCBs

Solution: Eliminate the chip package and reduce chip-to-chip spacing

WHAT IS A MULTICHIP MODULE (MCM)?

A collection of die attached to a high density interconnect structure which functions as a single integrated circuit.

[Diagram of Multichip Module (MCM)]
MCM ADVANTAGES

- Supports high pin count ICs without cost or performance penalty
- Improves performance
  - Low inductance (less than 2 nH/pin) and capacitance (better than 4x reduction)
  - Packaging delays for CMOS are reduced by at least 4 ns in most applications
  - Packaging delays for ECL are reduced by at least 2 ns in most applications
- Higher packing density (5 - 20x area reduction in most applications)

MICROPROCESSOR PERFORMANCE

<table>
<thead>
<tr>
<th>Year</th>
<th>MCMs with chip redesign **</th>
<th>MCMs *</th>
<th>Conventional packaging</th>
</tr>
</thead>
<tbody>
<tr>
<td>89</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>90</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>91</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>92</td>
<td></td>
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<td>93</td>
<td></td>
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<td>94</td>
<td></td>
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<td></td>
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<tr>
<td>95</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>96</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Assumes a 4 ns gain
** Assumes a 6 ns gain
nCHIP MULTICHIP MODULE TECHNOLOGY

- Interconnection Substrate
  - Base material - Silicon
  - Dielectric - SiO₂
  - Metallization - Aluminum or Copper
  - Passives (R, C)

- Assembly
  - Wire bond
  - Flip chip (1991)

- Package (Module Carrier)
  - Ceramic
  - Low cost non-hermetic (1991)

- Cooling
  - Air
  - Liquid

nCHIP SILICON CIRCUIT BOARD

- Wire Bond
- Reworkable Thermally Conductive Adhesive
- Si-nitride Passivation
- Terminating resistors (e.g., 50Ω)
- Two Signal Metal Layer
  - Aluminum (sputtered) or copper (electroplated)
- Silicon Dioxide Insulator
  - High thermal conductivity
  - Negligible moisture absorption
  - Simple, low cost process
  - Up to ~20 μm thick
  - Low-expansion, stress-controlled
- Power & Ground
  - Integral decoupling capacitor
- Silicon Base
  - High thermal conductivity
  - Thermal expansion match
nCHIP SUBSTRATE CHARACTERISTICS

<table>
<thead>
<tr>
<th></th>
<th>Type D</th>
<th>Type C</th>
<th>Type E</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Signal Layers</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Number of Power Layers</td>
<td>2</td>
<td>2</td>
<td>2-3</td>
</tr>
<tr>
<td>Max Wiring Density (mils/in²)</td>
<td>2000</td>
<td>1360</td>
<td>1000</td>
</tr>
<tr>
<td>Metal Pitch (μm)</td>
<td>25</td>
<td>37.5</td>
<td>50</td>
</tr>
<tr>
<td>Conducive Metal</td>
<td>Aluminum</td>
<td>Copper</td>
<td>Copper</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>3.5</td>
<td>3.5</td>
<td>3.5</td>
</tr>
<tr>
<td>Capacitance/nominal width (pF/cm)</td>
<td>1.2</td>
<td>1.2</td>
<td>0.65</td>
</tr>
<tr>
<td>Resistance</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>nominal width (Ω/cm)</td>
<td>15</td>
<td>3.8</td>
<td>1.6-2.2</td>
</tr>
<tr>
<td>1 mil width (Ω/cm)</td>
<td>5.9</td>
<td>2.3</td>
<td>1.0-1.4</td>
</tr>
<tr>
<td>Impedance/nominal width (Ω)</td>
<td>50</td>
<td>50</td>
<td>70</td>
</tr>
</tbody>
</table>

TEST SUBSTRATE

- Test substrate size is 2.73 cm x 2.21 cm and has 120 signal pads and 93 power and ground pads
- Verifies Electrical, Technology & Assembly characteristics and limits
- Variations of the basic design rules were implemented on three different substrates
  - 16 structures for delay and crosstalk measurement for both the interconnect layers
  - 12 structures which stress various aspects of the process technology like step coverage, minimum feature sizes, minimum spacing, etc.
  - 8 different structures, including test die, which are used for die attach and wire bonding tests
• **Type D**
  Simulated delay of 2 cm M3 line is 175 ps
  Measured delay of 2 cm M3 line is 184 ps

• **Type C**
  Simulated delay of 2 cm M3 line is 155 ps

• **Type D**
  Simulated delay of 10 cm M3 line is 850 ps
  Measured delay of 10 cm M3 line is 910 ps

• **Type C**
  Simulated delay of 10 cm M3 line is 692 ps
nCHIP WIRE BONDS HAVE LOW INDUCTANCE

In conventional IC packages, the wire bonds are used as space transformers.

The nCHIP bond pad pitch is matched to the IC chip.

• Wire bond lengths up to ~180 mils
• Resistance, inductance, and "sag" a problem
• Wire diameters must be large (~1.3 mil)

• Wire bond lengths 40-50 mils
• Inductance is low (1.2nH)
• Bond pitch can be fine (4 mils)

ROSS (SPARC) MODULE

• 5 VLSI components (0.8 micron), comprising a complete central processor chipset

• Normally packaged on a 3.3" x 7.25" PCB with a 100-pin connector

• Multi-die package version packaged in a single 224-pin CQFP

• Size of substrate is 0.93 in x 1.19 in (21x smaller in area than PCB)

• Contains 5 die (4 unique):
  - 292 x 330 mils, 196 pads
  - 420 x 393 mils, 166 pads
  - 421 x 445 mils, 244 pads
  - 337 x 269 mils, 50 pads

• 3 million transistors in total
BENEFIT OF nCHIP TECHNOLOGY FOR ROSS APPLICATION

- Higher performance
  - All chip-to-chip delays are under 1 nsec
  - Clock skew between chips is less than 200 psec
  - Eliminates package-induced ground bounce and simultaneous switching noise
- Comparable in cost to single chip packaging approach with higher density
SUMMARY

Single chip packaging solutions are becoming:
- More expensive due to increasing chip I/O
- More performance limiting due to increasing clock frequencies

nCHIP's MCM technology overcomes the limitations of single chip packaging solutions
- Supports high pin count ICs without cost or performance penalty
- Chip to chip delays are reduced to under 1 nsec
- Eliminates package-induced ground bounce