Experience
With the
Intel i860®

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Agenda
Why Couple the i860 and the i486®?

Hardware Requirements

Software Requirements

Customer Application Experience

Ideas for the Future

Summary
Why Couple the i860 and the i486?

Minicomputer applications moving down
May have used array processor with the minicomputer
Continued to do so in the PC implementation
Hardware too costly for broad market appeal
PC-type busses create performance bottlenecks
Need more integration for higher performance and lower cost

PC applications moving up
Developed an appetite for floating point
Possibly used a math coprocessor
Now running out of horsepower
Need high-performance numerics

Some Actual Applications
in the Image Processing Area

Screening Pap Smears for Pre-cancerous Cells
Printed Circuit Board Inspection
Low-end CAT scan
(Computerized Axial Tomography)
Some Actual Applications in non-Imaging Areas

Multi-axis robotic arm positioning system

Real-time quality control of hot-rolled steel

Neural-network processing of video data

Oil-field data analysis

General-purpose vector processing

Hardware Requirements

Viable Stand-Alone i486 Product
Implies low-cost infrastructure to support i860

Memory System
Wide range of sizes, including LARGE
Flexible sharing scheme

Application Freedom
Many configurations possible
Providing Low-cost Support for i486 and i860 Processors

Support i486 "Burst Mode" for Cache Fills

1-clock bursts imply a 64-bit physical DRAM system, with 2-way interleaving as seen by the i486

- i860 Requires 64-bit DRAM system •

64-bit Slot for local-bus expansion
Memory expansion, video card, supports "master-mode"

Standard I/O Subsystem for Economy
EISA Bus using commercial chip set
Bus folding buffers already exist, due to support of i486 bursts
32/64-bit Bus Structure

Providing a Wide Range of Memory Sizes

64-bit bus would require a minimum of 8 traditional "x9" SIMMs
Too much real estate, not enough range, only 3 sizes possible

Use 1 - 4 pairs of 36-bit JEDEC-standard SIMM modules
Allows from 2 to 64 Megabytes of DRAM on the MotherBoard

Providing for Flexible Sharing of Memory

Applications demand many options:
Privacy, sharing, write protect, etc.

Use a very fast SRAM for address decode,
this allows for dynamic configuration
Providing for Cache Coherency of Shared Data

Additional complication when sharing:
- 486 snoops bus for cache coherency, 860 does not
- Configure shared area as cached for 486, not cached for 860

Memory Map Scheme as Seen by Software

Distinct attributes for each 32K of each processor's address space
- Read/Write --- Read Only
- Cacheable --- Not Cacheable
- Fast DRAM --- Slow DRAM

DRAM Enabled --- No DRAM (usually I/O system)
Select SIMM Module Pair 0/1/2/3, Front/Back
Allows flexibility in sharing, exclusion, cache strategy, etc.

Mapping SRAM Diagram
Application Freedom

Complete Symmetry in Memory Access
- 1486 and 1860 have common page table formats, no extra work needed here

The 1860 has no I/O instructions
- Dedicate an address range to I/O cycles, 1860 access to C2000000-C200FFFF

Both processors have local caches, both will signal "bus request" when in HOLD, I/O system issues HRQ when DMA is desired
- One PLD acts as a programmable central arbiter

Either processor may need to handle interrupts
- Design 1860 interrupt control PLD, I/O system hangs off one chain, software-initiated cross-processor interrupts also implemented

Bus Arbitration PLD Diagram
Software Requirements

i486 Systems using the i860 as an Applications Accelerator

Program runs on i860, uses i486 for I/O processing
May involve Intel’s APX860 kernel for portability, ease of use

Program runs on i486, uses i860 for compute-intensive tasks
Typically requires custom programming, "Remote Procedure Call" model

Stand-alone i860 Workstations

Typically running UNIX860
Possible use of i486 to run a "DOS Window"
APX860 System Configuration
UNIX-host version currently available from Hauppauge, DOS-host version under development

UNIX 386
DEVICE DRIVERS

USER SOFTWARE
486 UNIX PROCESS 860 SBS-COMPLIANT PROCESS

EISA I/O SYSTEM

APX

64-Bit FRAME BUFFER

Hauppauge Computer Works, Inc.

UNIX860 System Configuration
Under development, not yet commercially available - shown running with 64-bit Frame Buffer and XWindows at Uniforum in January 1990

USER SOFTWARE
8088 DOS PROGRAMS 860 UNIX PROCESS

DOS COMPATIBILITY SOFTWARE

X WINDOWS

UNIX 860

EISA I/O SYSTEM

64-Bit FRAME BUFFER

Hauppauge Computer Works, Inc.
Ideas for Future Development

Alliant/Intel PAX-compatibility plug-in module
- Gives the i860 something to talk to in the WeiTek socket
- Implements single-CPU version of Concurrency Control

64-bit RAM card - probably 64/256 Megabyte

Master-mode Multiprocessor plug-in card
for 64-bit slot

Working with the i860

Summary

Highlights
- Areas of compatibility between i486 and i860, such as page tables, data formats, address range
- Attractive balance of integer/floating point power

Lowlights
- i860 signal timing is not as tight as the i486, resulting in less margin and harder design
- Chip bugs in early versions of i860
  (details are not for group discussion)