Get Off the Bus and Call A TAXI

Hot Chips Symposium II  August 21, 1990

PAUL SCOTT
Design Engineering Manager
Network Products Division
Advanced Micro Devices

GET OFF THE BUS AND CALL A TAXI

BUS INTERCONNECTS CAUSE COMMUNICATION BOTTLE-NECKS
TAXI™ LINKS CREATE PRIVATE SERIAL DATA CHANNELS
PRIVATE SERIAL LINK PROBLEMS

Challenges

SYSTEM ARCHITECTURE COMPATIBILITY

SERIAL LINK BANDWIDTH

INTEGRATION OF CLOCK GENERATION & RECOVERY

MANY DATA TRANSMISSION RATES

APPROPRIATE INTERCONNECT MEDIA & INTERFACE

TECHNOLOGY FOR CHIP DESIGN & MANUFACTURE

MINIMUM BOARD SPACE REQUIREMENT

AMD

TAXIchip™ SYSTEM BLOCK DIAGRAM

Transparent Asynchronous Xmitter/Receiver Interface

Parallel Input

HOST DATA SOURCE

FLOW & CONTROL SOURCE

Serial Transmission Link

TRANSMITTER

Am766-125
Am766-176
Am7916-128
Am766-40
Am7916-260
Am7928-600
Am793336-1600

SERIAL RATE (kbps)

40-125
125-176
40-125 (QPSK)
8-40
200-280
480-620
1020-1920

RECEIVER

Am766-125
Am766-176
Am7916-128
Am766-40
Am7916-260
Am7928-600
Am793336-1600

AVAILABLE

Production NOW
Production NOW
Samples 90-04
Samples 90-04
Samples 91-04
Samples 91-01

Parallel Output

HOST DATA DESTINATION

FLOW & CONTROL MONITOR

AMD
TAXI PARALLEL INTERFACE

SIMPLE TO USE AS AN OCTAL REGISTER

AUTOMATIC MUX/DEMUX DATA & COMMAND

TAXI CODES FACILITATE DATA TRANSFERS

ENCODER EFFICIENCY DETERMINES BANDWIDTH REQUIREMENT

'OUT-BAND-SIGNALS' ENHANCE LINK BANDWIDTH

CODE CHARACTERISTICS DEFINE LINK LIMITATIONS

RESULT

4B/5B & 5B/6B CODES ≤20% OVERHEAD

8, 9, 10 BIT DATA BYTES

4, 3, 2 BIT COMMAND SYMBOLS

CODES SUPPORT NETWORK STANDARDS
TAXI SERIAL OUTPUT

INTERNAL PLL GENERATES BIT CLOCK FROM EXTERNAL BYTE FREQUENCY
ENCODER ASSURES EFFICIENT DATA TRANSFER WITH HIGH TRANSITION DENSITY

TAXI TRANSMITTER

TAXI SERIAL INPUT

INTERNAL PLL SYNCHRONIZES BIT CLOCK WITH INCOMING SERIAL STREAM
DECODER SEPARATES DATA FROM COMMAND AND FLAGS ERRORS

TAXI RECEIVER
TAXI SERIAL INTERFACE

ECL 100K OUTPUTS INTERFACE TO STANDARD OPTICAL MODULES
LOW IMPEDANCE DRIVERS CAN DRIVE LONG TRANSMISSION LINES

TAXI TRANSMITTER

OPTICAL INTERFACE MODULE

REMOTE TAXI RECEIVER

SINGLE ENDED or DIFFERENTIAL
ALL COMMON WIRE MEDIA INCLUDING COAX and TWISTED PAIR

TAXI SERIAL INTERFACE

DIFFERENTIAL INPUT COMPATIBLE WITH STANDARD OPTICAL MODULES
HIGH SENSITIVITY AND WIDE COMMON MODE RANGE ENCOURAGE WIRE INTERCONNECT

REMOTE DRIVER

TRANSMISSION LINE IMPEDANCE = Z0

SINGLE ENDED or DIFFERENTIAL
ONE-WAY or BIDIRECTIONAL USING SIMPLE PASSIVE BRIDGE.
LINK LENGTH LIMIT

BANDWIDTH LIMITED LINKS (COAX) CAUSE JITTER IN NORMAL DATA
JITTER LIMITS THE LINK LENGTH BEFORE THE AMPLITUDE LIMIT

TAXIchip LINE LENGTH

TRANSMISSION LINE CHARACTERISTICS LIMIT LENGTH
EACH TYPE HAS DIFFERENT ECONOMIC & PERFORMANCE TRADEOFFS
TAXIchip POWER BUS PARTITION

TTL & ECL I/O NOISE ISOLATED FROM CORE BY BUS SEPARATION
INTERFACES BETWEEN I/O AND INTERNAL LOGIC & PLL ARE DIFFERENTIAL
INTERNAL CURRENT TRANSIENTS CREATE NOISE VOLTAGES IN LEAD INDUCTANCE
CML AND PLL CIRCUITS CAUSE MINIMAL INTERNAL NOISE

TAXIchip PRODUCT PARTITION

REDUCE DATA CORRUPTION CAUSED BY CROSSTALK
MINIMIZE INTERFACE DATA RATE
SELECT BLOCKS FOR EFFICIENT, MANUFACTURABLE INTEGRATION
MINIMIZE CHIP COUNT AND INTERFACE PIN COUNT
TAXIchip SERIAL LINK SOLUTIONS

FLEXIBLE SYSTEM INTERFACE
DRIVES TRANSMISSION LINES or OPTICAL MODULES
PLLs WITH NO EXTERNAL COMPONENTS
INTERNAL BIT RATE CLOCK GENERATOR
INTEGRATED CLOCK/DATA RECOVERY PLL
WIDE FREQUENCY RANGE
MATURE IC TECHNOLOGY FOR MANUFACTURABILITY

AMD

TAXIchip SPEED LIMITS
TAXIs ADDRESS SPECIFIC DATA COMMUNICATION REQUIREMENTS
SPEEDS DEFINED BY INTERFACE LIMITATIONS AND SYSTEM CONVENTIONS
PRODUCTS PARTITIONED FOR COST EFFECTIVE SYSTEM SOLUTIONS

<table>
<thead>
<tr>
<th>Product</th>
<th>Data Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Am79268/269</td>
<td>450-500 Mbaud</td>
</tr>
<tr>
<td>Am79168/UR</td>
<td>200-250 Mbaud</td>
</tr>
<tr>
<td>Am79G368/369</td>
<td>&gt; 1500 Mbaud</td>
</tr>
</tbody>
</table>

TAXI DATA RATE (Mbaud)