August 26, 1991—Memorial Hall Auditorium

8:30 – 8:45  Welcome and Opening Remarks
Martin Freeman, General Chair
Forest Baskett and John Hennessy, Program Co-Chairs

8:45 – 10:15  Session 1: High-Performance Processors – 1
Session Chair: John Hennessy, Stanford University
- SuperSPARC™: A Fully Integrated Superscalar Processor
  Greg Blanck, Sun Microsystems
  Steve Krueger, Texas Instruments
- MIPS R4000 Technical Overview
  Earl Killian, MIPS Computer Systems
- PA-RISC Processor for "Snakes" Workstation
  Charles Kohlhart, Hewlett Packard

10:15 – 10:45  Break

10:45 – 12:15  Session 2: Highly Parallel Chips
Session Chair: Martin Freeman, Philips Research
- The LIFE Family of High-Performance Single Chip VLIWs
  Gerrit Slavenburg and Yen Lee, Philips Research Palo Alto
  Andrew Huang, CMU
- The Message-Driven Processor
  William Dally, J. Stuart Fiske, Waldemar Horwat, John Keen,
  Richard Lethin, Michael Noakes and Peter Nuth
  MIT Artificial Intelligence Laboratory
  D. Scott Wills, University of Central Florida
  Andrew Chien, University of Illinois
  Salim Ahmed, Paul Carrick, Roy Davison, Greg Fyler
  Steve Lear, Mark Vestrich and Teg Nguyen, Intel
- The TRW CPUAX Superchip
  A. Miscione, R. Almeida, H. Hennecke and R. Mann
  TRW Electronics and Technology Division

12:15 – 1:45  Lunch at Wilbur Hall Canopy

1:45 – 3:15  Session 3: High-Performance Processors – 2
Session Chair: Forest Baskett, Silicon Graphics
- An 80 MHz 64-Bit Floating Point RISC Processor
  with Direct DRAM Support
  James Hesson, Micron Technology
- The 1860™ XP: 2nd Generation of the 1860™
  Supercomputing Microprocessor Family
  David Perlmutter and Michael Kagan, Intel Israel
- Beyond Claims of Free Transistors and Abundant
  Instruction-Level Parallelism
  Michael Smith, Stanford University

3:15 – 3:45  Break

3:45 – 5:15  Session 4: Low Power and Low Cost
Session Chair: Alan Smith, U.C. Berkeley
- Tera microCORE Chipset
  Greg Favor, Tera Microsystems
- The SparKIT™ Chipset
  Mohammed Wasfi, LSI Logic Corporation
- SPARC® Modules
  Raju Vegesna, Ross Technology

5:15 – 7:15  Reception at Wilbur Hall Canopy

7:30  Evening Panel Session
Five Instructions Per Clock: Truth or Consequences
Session Chairs: Alan Smith, U.C. Berkeley and John Mashey, MIPS
  Computer Systems
Panelists: Joseph A. Fisher, Hewlett Packard Laboratories; Norm Jouppi,
  DEC Western Research Lab; Monica Lam, Stanford University; James
  Smith, Cray Research; David Wall, DEC Western Research Lab
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9:00 — 10:30 Session 5: Communications
Session Chair: Teresa Meng, Stanford University
• A GaAs 200 Mbps 64x64 Crosspoint Chip
  Ron Cates, Vitesse Semiconductor
• An Enhanced Crossbar Router Chip for a Shared Memory
  Multiprocessor
  Henry Minsky, Tom Knight and André DeHon, MIT AI Lab
• The NEURON Chip Family Architecture
  Robert Dolin, Echelon
• The Protocol Engine Chipset
  Des Young, Protocol Engines

10:30 — 11:00 Break

11:00 — 12:30 Session 6: Caches and Floating Point
Session Chair: John Crawford, Intel
• MIPS R4000 Caches and Coherency
  Paul Ries, MIPS Computer Systems
• The Megacell Differentiated Floating Point Product Family
  Merrick Darley, Don Steiss, Peter Groves, David Bural
  Maria Gill and Tod Wolf, Texas Instruments
• 82495DX/82490DX: A High-Performance 2nd Level Cache
  for the 1486™ DX CPU
  Adi Gobert, Intel Corporation

12:30 — 2:00 Lunch at Wilbur Hall Canopy

2:00 — 3:30 Session 7: Special Processors
Session Chair: John Mashey, MIPS Computer System
• A Smart Frame Buffer
  Joel McCormack, DEC Western Research Laboratory
  Bob McNamara and Lindsay Gage, DEC
• CNAPS (Connected Network of Adaptive ProcessorS)
  Dan Hammerstrom and Gary Tahara, Adaptive Solutions
• SMM, The "Virtual 386™"
  Dave Vannier, Intel

3:30 — 4:00 Break

4:00 — 5:00 Session 8: High-Performance Processors — 3
Session Chair: Dave Ditzel, Sun Microsystems
• National's Swordfish — A Superscalar with DSP
  Reuven Marko and Motti Beck, National Semiconductor
• T9000 — Superscalar Transputer
  Bob Krysiak, Richard Forsyth and Roger Shepherd
  INMOS Ltd. — SGS-Thomson Microelectronics

5:00 Closing Remarks

Organizing Committee
General Chairman:
Martin Freeman, Philips Research
Program Co-Chairmen:
Forest Baskett, Silicon Graphics
John Hennessy, Stanford University
Treasurer:
Hasan AlKhatib, Santa Clara University
Registration Chairman and
Local Arrangements Chairman:
Robert Stewart, Stewart Research
Publicity Chairman:
Andre Goforth, NASA Ames Research Center
Publication Chairman:
Nam Ling, Santa Clara University

Program Committee
Co-Chairmen: Forest Baskett, Silicon Graphics
John Crawford, Intel
David Ditzel, Sun Microsystems
John Mashey, MIPS Computer Systems
John Hennessy, Stanford University
Teresa Meng, Stanford University
Alan Smith, U.C. Berkeley