Super SPARC™
A Fully Integrated Superscalar Processor

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Program Objectives

Workstation Microprocessor Essentials

- High Performance
- 100% Application Binary Compatible
- High Integration
- Useful in Several Configurations
- Extensive Test/Debug Support

Super Sparc Solution

- 3 Instruction Resource-Rich SuperScalar
- Fast Double-Precision Floating Point
- Single Cycle Loads/Stores
- BICMOS
- SPARC Version 8 Architecture (IMUL/IDIV)
- IU/FPU/MMU/Cache/Mbus on-chip
- All Fully MP "ready"
- Large Internal Caches
- Companion Cache Controller
- Built-in Self Test
- JTAG Scan Based Emulation
- ICE-like debugging features
Super SPARC™

- High Performance, Superscalar
- Highly Integrated
- 3.1 million transistors, BiCMOS
- 3 Instructions/Cycle Issue and Execution
- SPARC Version 8 Compatible
- Direct MBus Level II or used with External Cache Controller
- Optional External Cache Controller
- Fully integrated, on-board cache tags
- Synch or Async interface to system bus
- 1MB unified, direct-mapped cache
- MBus Level-II Interface
  (Cache Consistent Multiprocessor Interconnect)

Super SPARC™

- Floating Point Control
  - Complete Double Precision
  - No Unfinished Operations
- Integer Unit Control
  - Instruction Grouping/Decode
  - 128 bit Access
- MMU
  - 64 Entry Fully Associative
  - 4-way set associative
  - 64 bit Access
- Data Cache
  - Physically Addressed
  - 16 KByte
  - 4-way set associative
- Dual System Interface
  - MBus Level II
  - Viking Bus to External Cache
  - MBus Level I Buffer
  - Store/Copyback

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Super SPARC™

MBus Configurations

Lower Cost Systems

Higher Performance Systems

Super SPARC™

Superscalar Principles of Operation

- 3 instruction/cycle issue & execute, fully dynamic scheduling
- Simultaneous execution may be constrained by:
  - data dependencies
  - control dependencies
  - internal resources
- SuperSPARC Resources:
  - Single 64-bit LD/ST
  - Two 32-bit ALUs
  - Single FP Issue
  - Single Br/Jmp/Call/Return
  - Two 32-bit integer results
- Designed to handle dependencies well, not wish them away
Superscalar Example

```assembly
ldd [%10],%f2
fadd %f2,%f0,%f6
add %10,0x8,%10
! -- Break (Three Instructions max)
ldd [%10],%f4
add %10,0x4,%10
fmuld %f4,%f0,%f8
! -- Break (Three Instructions max)
ldd [%10+4],%f10
cmp %10,0x100
be Loop
! -- Break (Branch, Three Instructions)
```

MBus Multiprocessing

- SuperSPARC has complete multiprocessing support
- First and optional second level caches all coherent
- MBus interface has snoop logic
- Processor not affected by most snoop traffic
- System configuration, memory speed and applications, limit number of processors that can be supported
- Supports SPARC Architecture Version 8 multiprocessor memory model (Total Store Ordering and Partial Store Ordering)
Technology

• SuperSPARC CPU and Cache Controller are manufactured in TI's EPIC IIIB process
  - 0.8 micron minimum feature size
  - BiCMOS - Best of Bipolar and CMOS circuits
    Bipolar: I/O and interconnect
    CMOS: Density and simplicity
  - Triple Level Metal

• High Performance Dense Ceramic Pin Grid Array (CPGA) with heatsink
  - SuperSPARC CPU: 293 pins, 70 mil pin to pin
  - SuperSPARC CC: 369 pins, 70 mil pin to pin

Summary

• 3 instruction Superscalar groups and schedules instructions

• High integration of critical features gives higher performance at lower cost

• BiCMOS for the right balance of speed, density and simplicity

• MBus "multiprocessing ready"

• SPARC Architecture Version 8: 100% binary compatible