RISC Chipset Technology for the 1990s

Tera microCORE Chipset

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Tera microCORE Chipset

- Most highly integrated SPARC chipset available
- Integrates cache, memory management, DRAM control, I/O, color video display control, and Sbus interface into four components
- Reduces component count of SPARC-compatible system by 50%
- Supports laptop or SLC-class machine with minimal two-chip configuration
- 25/33/40 MHz frequencies
- 1.0 μ and 0.8 μ CMOS technologies
Architectural Goals

- Minimize component count
- Allow QFP packaging option
- Simplify board design
  - VLSI building blocks, no glue
  - Easy high frequency operation
System Controller (SCU)

- **Direct interface to SPARC integer/floating point unit**
  Weitek, Cypress/Ross, Fujitsu, LSI Logic
- **Instruction and data caches**
  4KB/4KB, physical, direct-mapped, write-through
- **Write buffer**
  8 words deep; byte and doubleword merging
- **SPARC Reference MMU**
  64-entry fully-associative TLB, hardware TLB miss handling
- **Memory controller**
  Up to 64 MB of DRAM, 2-way & 4-way page interleaving, SRAM/EPROM support
- **microBUS controller**
  Multiplexed 36-bit address/data, centralized arbitration
- **224-pin CPGA, 224-pin PPGA**

I/O Controller (IOC)

- **Direct interface to Ethernet controller**
  Buffered interface to AMD Lance, block transfers to/from memory
- **Direct interface to SCSI controller**
  FIFO-buffered interface to NCR/Emulex 53C90 + DMA
- **Direct interface to 8 byte-wide peripheral & memory devices**
  Programmable interface, 3 undedicated DMA channels
- **Monochrome video display controller**
  Resolutions up to 1280x1024, DRAM-based frame buffer, h/w cursor
- **Internal peripherals**
  Interrupt controller, 3 counter/timers, 2 serial ports
- **208-pin PPGA, 208-pin QFP**
Reasons for Integrating Cache Memory

- Component count
  Eliminates external SRAMs
- Cost
  Eliminates high-speed SRAMs
- Physically-addressed cache
  Software-transparent cache consistency
- Overlapped CPU execution/cache Fill
  Requested word returned first; early CPU release; streaming mode
- Scalability to higher frequencies
  Critical timing within a single chip
- Lower miss penalty
  4-7 cycles vs. 13 cycles for SPARCstation1, 26 cycles for SPARCstation2

Comparison with SPARCstation 1 External Cache

<table>
<thead>
<tr>
<th></th>
<th>External 64KB DM</th>
<th>Integrated 4KB, 4KB, DM</th>
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</thead>
<tbody>
<tr>
<td>I-Miss Ratio</td>
<td>3.6% (Unified)</td>
<td>9.4%</td>
</tr>
<tr>
<td>D-Miss Ratio</td>
<td>n/a</td>
<td>11.0%</td>
</tr>
<tr>
<td>Miss Penalty</td>
<td>13*</td>
<td>5.5</td>
</tr>
<tr>
<td>CPI Penalty</td>
<td>0.59</td>
<td>0.67</td>
</tr>
<tr>
<td>CPI</td>
<td>-2.00</td>
<td>-2.08</td>
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<tr>
<td>Performance</td>
<td>Baseline</td>
<td>-4%</td>
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* Note: SPARCstation 2 has 26 cycle miss penalty
Both assumes 1.25 references/instruction
For Tera: 60% page hit rate, 4 cycles to first word on page hit
           7 cycles to first word on page miss
microBUS...

...the most cost-effective memory interconnect

- Low pin count results in:
  - Die area reduction
  - Power reduction
  - QFP packaging
- Balanced CPU/memory bandwidth
- Simple bus protocol
- 111 Mbytes/sec at 33 MHz - suitable for uniprocessing
- Support for innovative virtual DMA implementation

Direct Memory Access

- Physical DMA - hardware or software chaining to support paged, virtual memory environment
- Virtual DMA - all I/O traffic passes through the MMU
  - Simplifies hardware
  - Memory protection for free
  - Lower software overhead
- Tera Virtual DMA
  - Avoid MMU and/or bus bottlenecks
  - Applies to all bus masters
Distributed Address Translation

- Request is serviced by the PTLB; may require table walk by the ATP
- Mini-TLB miss requires PTLB address translation request
- Translation returned as read data

Video Display Controller (CXP)

- Integrates frame buffer controller and video display controller
- 8-bits per pixel color and gray-scale displays
- Programmable display resolutions up to 1280 x 1024
- No external glue logic - only RAMDAC and VRAMs
- Programmable video timing
- 32x32 two bits per pixel hardware cursor (X-compatible)
- 160-pin PPGA, 160-pin QFP
**SBus Expansion Interface (BXP)**

- Implements the full SBus B.0 specification
- Supports up to 4 SBus slots
- Handles transactions from the Memory Bus to SBus, from SBus to the Memory Bus, and between two SBus devices
- Dual 64 and 128-byte FIFO data buffers
- Asynchronous interface allows maximum 25 MHz SBus frequency, independent of system clock frequency
- 64-entry SPARC Reference TLB
- Integrated interrupt controller
- 208-pin PPGA, 208-pin QFP

**Competitive Advantage**

- Optimized for low-cost systems
- Simple board design
  - No external high-speed SRAMs required
- Frequency Scalability
  - Critical timing internal to System Controller Unit
- Highly Integrated Solution
  - Space & Power savings
  - Higher reliability
  - Lower manufacturing cost
- Components suited for a wide range of designs