An Enhanced Crossbar Router Chip for a Shared Memory Multiprocessor

- A "RISC" approach to router chip architecture and design
- High performance system engineering
- How simple can we make it?

Transit Target Specifications

- 256 Processor / Memory clusters
  - expandable with fat tree techniques
- 8 bit parallel transfers
  - one additional control line per port
- 100 Megabytes/sec/port
- 220 ns. remote memory reference
- Robust against single point failures
- Compact - 50 x 50 x 5 cm
The "RISC" Approach To Routing

- Amazingly simple network protocol gives flexibility to system designers
- Logic is simplified, speeded up
- Wiring topology of network combined with router dilation gives good collision statistics
- No external components needed to cascade chips in network
Multipath Bidelta Network

16 x 16 Bidelta Network Constructed from 4 x 2 Crossbars with a Dialation of 2
Transit Routing Protocol

- Circuit Switched
- Source Responsible Routing
- Explicit Acknowledgement
- Simple
  - No buffering
  - No queuing
  - No flow control
- Non-Deterministic Paths
- Fault Tolerant
- Fault Localization
Transit Routing Protocol

Forward data:
- I = idle byte
- R = routing byte
- D = data byte
- T = turn
- X = drop
- S = status
- C = checksum

Backward data:
- S
- C
- D
- D
- D
- X
- T

RN1 Crossbar Chip

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Allocate Grant Chain

A Dilated output column.
Channel 1 is the Primary, Channel 2 is the secondary.
Packaging of Transit

- True Three Dimensional wiring
  - Roughly constant wiring density in all three axes (within factors of 5)
- Laminated stack of alternating layers of components and horizontal wiring
- Dense Connectors made from Fuzz Buttons
- Controlled Impedance 50 Ohm stripline wiring
- Fluid cooling - Fluorinert
- Dominant Signal Flow is Vertical
- Each wiring / component layer is identical

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Logical Diagram of Simplified Network

From Processing Nodes

Network Inputs

Network Outputs

To Processing Nodes

(Networks not drawn to scale.)

Physical Network Construction

From Processing Nodes

Network Inputs

Routing Stack

Routing components are distributed evenly in both dimensions across each plane.

To Processing Nodes

To Processing Nodes

(printed circuit board)