THE MEGACELL DIFFERENTIATED FLOATING POINT PRODUCT FAMILY

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AGENDA

- FLOATING POINT FAMILY STRATEGY
- METHODOLOGY
- BENEFITS
- MEGACELLS
- FIRST IMPLEMENTATION
- SUMMARY
FLOATING POINT FAMILY STRATEGY

- IEEE 754 FLOATING POINT STANDARD
- DOUBLE PRECISION DATAPATHS
- PROPRIETARY LOW LATENCY ALGORITHMS
- SUPPORT INTEGER FORMATS
- SUPPORT LOGIC OPERATIONS
- FLEXIBILITY TO VARY CLOCK FREQUENCY, THROUGHPUT, AND LATENCY TO MEET SYSTEM NEEDS

METHODOLOGY

- KEY DATAPATH AND MEMORY MEGACELLS ARE DESIGNED IN FULL CUSTOM
- "C" MODELS FOR EACH MEGACELL ARE AVAILABLE FOR SIMULATION
- CUSTOMER IS PROVIDED WITH PROCESS COMPATIBLE GATE ARRAY TECHNOLOGY
- SYSTEM SPECIFIC LOGIC IS DESIGNED BY CUSTOMER
- GATE ARRAY NETLIST IS ROUTED AT TI TO DESIRED ASPECT RATIO
- I/O'S, GATE ARRAY, AND DESIRED MEGACELLS ARE COMBINED IN A CUSTOM ENVIRONMENT
BENEFITS

- MEGACELLS PROVIDE FULLY COMPACTED, HIGH PERFORMANCE DATAPATHS AND MEMORY UNITS
- GATE ARRAY PROVIDES EASE OF USE AND QUICK-TIME-TO-MARKET FOR CUSTOMER SPECIFIC LOGIC
- CUSTOMER'S RESOURCES ARE FOCUSED ON THEIR SYSTEM NEEDS
- TI'S DESIGN RESOURCES ARE FOCUSED ON THE MEMORY AND DATAPATH ELEMENTS AS WELL AS THE DEVICE TECHNOLOGY
- SUPPORTS SCALAR, PIPELINE AND SUPER PIPELINE ARCHITECTURES
- CONFIGURATION TO OPTIMIZE COPROCESSOR, PARALLEL PROCESSOR AND GRAPHIC ARCHITECTURAL SUPPORT
- HIGH PERFORMANCE LOW POWER 0.8 NM PROCESS

MEGACELLS

- DOUBLE PRECISION ALU
- SINGLE PRECISION ALU
- DOUBLE PRECISION MULTIPLIER
- SINGLE PRECISION MULTIPLIER
- VARIOUS REGISTER FILES
- DATA CACHE
- INSTRUCTION CACHE
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ALU AND MULTIPLIER MEGACELLS

- COMPATIBLE WITH IEEE STANDARD 754 FOR ADDITION, SUBTRACTION, MULTIPLICATION, DIVISION, SQUARE ROOT
- EACH MEGACELL IS TOTALLY INDEPENDENT WITH SEPARATE INSTRUCTION, DATA, AND STATUS BUSSES
- STATUS, CONTROL, AND DATA REGISTERS ARE PIPELINED IN PARALLEL
- MULTIPLIER CONTAINS A SEPARATE SEQUENCER
- GLOBAL COMMUNICATION WITH EACH OTHER DIRECTLY OR THROUGH REGISTER FILE
- DURING MULTICYCLE OPERATIONS THE SEQUENCERS WILL ASSERT SIGNALS THAT CAN BE USED TO STALL THE EXTERNAL INSTRUCTION STREAM
- ALL INTERNAL REGISTERS ARE SCANABLE
- DUAL MACHINE CAPABILITY OR NONDESTRUCTIVE SCAN CAPABILITY
- ALL INTERNAL REGISTERS CAN BE HALTED OR MADE TRANSPARENT

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MEGACELL

INSTR

A

B

INSTR_DECODER

OPER_PROCESSOR

CONTROL_PATH

DATA_PATH

STATUS_PATH

INSTR_OUT

RESULT

STATUS_OUT

CLOCK
MEGACELL FLOATING POINT NUMBER FORMATS

- NORMAL
- DENORMAL
- ZERO
- INFINITY
- SIGNALING NANS
- QUIET NANS
- 32-BIT SINGLE PRECISION
- 64-BIT DOUBLE PRECISION
- 80 AND 128-BIT EXTENDED PRECISION FOR PRIMITIVE OPERATIONS
- SIGNED INTEGERS
- UNSIGNED INTEGERS

ALU MEGACELL

- 64-BIT MANTISSA PROCESSING
- 12-BIT EXPONENT PROCESSING
- ALL INSTRUCTIONS ARE SINGLE CYCLE EXCEPT INTEGER DIVISION
- OPERATIONS CAN BE SPECIFIED IN THE GENERAL FORM:
  { +, -, ||, -|| } A OP { +, -, ||, -|| } B
- DENORMAL NUMBERS ARE PROCESSED IN TWO WAYS:
  IEEE MODE - GRADUAL UNDERFLOW
  FAST MODE - CONVERT TO ZERO
# ALU MEGACELL INSTRUCTIONS

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>FUNCTION</th>
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<tr>
<td>ADD</td>
<td>FLOATING POINT AND INTEGER ADDITION</td>
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<tr>
<td>ADDO</td>
<td>FLOATING POINT AND INTEGER ADDITION AND ZERO TO A OPERAND (CAN GENERATE ABS, NEG, -ABS)</td>
</tr>
<tr>
<td>ADDC</td>
<td>INTEGER AND WITH CARRY</td>
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<tr>
<td>AND</td>
<td>LOGICAL AND</td>
</tr>
<tr>
<td>SHIFTRA</td>
<td>ARITHMETIC SHIFT RIGHT BY N</td>
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<tr>
<td>CIC</td>
<td>CLEAR INTEGER CARRY</td>
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<tr>
<td>CLASS</td>
<td>NUMBER CLASS FUNCTION</td>
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<td>CMP</td>
<td>COMPARE AND SET STATUS</td>
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<td>SINGLE CYCLE FORMAT CONVERSIONS</td>
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<tr>
<td>IDV2</td>
<td>UNSIGNED INTEGER DIVIDE STEP 2</td>
</tr>
<tr>
<td>IDV1/2</td>
<td>UNSIGNED INTEGER DIVIDE ITERATE</td>
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<td>IDV1/4</td>
<td>UNSIGNED INTEGER DIVIDE TERMINATE</td>
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<td>IDV1/8</td>
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<td>EXE</td>
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<td>EXM</td>
<td>EXTRACT MANTISSA</td>
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<tr>
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<td>LOAD ALU MODE REGISTER</td>
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<td>SHIFTRL</td>
<td>LOGICAL SHIFT RIGHT BY N</td>
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<td>MERGEF</td>
<td>MERGE EXPONENT AND MANTISSA</td>
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<tr>
<td>NAND</td>
<td>LOGICAL NAND</td>
</tr>
<tr>
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<td>NO OPERATION INSTRUCTION</td>
</tr>
<tr>
<td>NOR</td>
<td>LOGIC NOR</td>
</tr>
<tr>
<td>OR</td>
<td>LOGICAL OR</td>
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<tr>
<td>PASSAQ</td>
<td>PASS WITH NO STATUS FLAGS, (CAN GENERATE FLOATING POINT ABS, NEG, -ABS)</td>
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<tr>
<td>PENC</td>
<td>PRIORITY ENCODE INTEGER</td>
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<tr>
<td>SIC</td>
<td>SET INTEGER CARRY</td>
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<td>SHFTR</td>
<td>SHIFT LEFT BY N</td>
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<tr>
<td>XNOR</td>
<td>LOGICAL XNOR</td>
</tr>
<tr>
<td>XOR</td>
<td>LOGICAL XOR</td>
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</table>

## ALU DATAPATH

- **Operand Processor**
  - APO
  - AP0

- **Operand Swapper**
  - Right Barrel Shifter

- **Normalization Predictor**
  - Adder
  - AP1

- **Left Barrel Shifter**
  - Correction Shifter

- **Incrementer**
  - Output Formatter
  - AP2
MULTIPLIER MEGACELL

- OPERATIONS CAN BE SPECIFIED IN THE GENERAL FORM:
  \( \{ +, -, ||, \lll a \} \text{ OP } \{ +, -, ||, \lll b \} \)

- DENORMAL NUMBERS ARE PROCESSED IN THREE WAYS:
  IEEE MODE – GRADUAL UNDERFLOW
  FAST MODE – CONVERT TO ZERO
  WRAP MODE – MULTIPLIER ACCEPTS AND PRODUCES WRAPPED NUMBERS AS OPERANDS AND RESULTS

- HIGH SPEED SUM OF PRODUCTS OPERATIONS CAN BE ACHIEVED IN COMBINATION WITH THE ALU

MULTIPLIER MEGACELL INSTRUCTIONS

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>FUNCTION</th>
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<tbody>
<tr>
<td>NOPM</td>
<td>NO OPERATION INSTRUCTION</td>
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<td>PASS A, NO STATUS UPDATE</td>
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<tr>
<td>MULT</td>
<td>MULTIPLY (MICROCODED EXCEPTIONS)</td>
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<tr>
<td>MULT1</td>
<td>MULTIPLY BY ONE (MICROCODED EXCEPTIONS)</td>
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<td>DIV</td>
<td>FLOATING POINT DIVIDE (MICROCODED)</td>
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<tr>
<td>INV</td>
<td>FLOATING POINT RECIPROCAL OF B (MICROCODED EXCEPTIONS)</td>
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<td>SQRT</td>
<td>FLOATING POINT SQUARE ROOT (MICROCODED)</td>
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<td>AINV/SQRTB</td>
<td>1 / SQRT(B)</td>
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<td>LMRM</td>
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MULTIPLIER MEGACELL THROUGHPUT

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<th>INSTRUCTION</th>
<th>THROUGHPUT IN CLOCK CYCLES</th>
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<td>64X64 INTEGER MULTIPLY</td>
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<td>UPPER HALF OR LOWER HALF</td>
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<tr>
<td>128-BIT RESULT</td>
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<tr>
<td>IEEE FLOATING POINT MULTIPLY</td>
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<tr>
<td>IEEE FLOATING POINT SQRT</td>
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<tr>
<td>FLOATING POINT 1/SQRT</td>
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<tr>
<td>SINGLE</td>
<td>5</td>
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<tr>
<td>DOUBLE</td>
<td>6</td>
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</table>

MPY DATAPATH

- Operand Processor
- MPO
- Operand Routing Network
  - 64x32 Parallel Multiplier
  - 64x32 Parallel Multiplier
- Div/Sqrt Registers
- Signed-Digit Adder
- MP1
- Signed-Digit to Binary Converter
- Rounding Selector and Output Formatter
- MP2
REGISTER FILE MEGACELL

- 32-DEEP BY 64-BIT WIDE
- LONG-WORD ADDRESSABLE
- STORE 64 SINGLE PRECISION OPERANDS OR 32 DOUBLE PRECISION OPERANDS
- 2 READ PORTS AND 1 WRITE PORT DEDICATED TO THE ALU
- 2 READ PORTS AND 1 WRITE PORT DEDICATED TO THE MULTIPLIER
- 1 READ PORT AND 1 WRITE PORT DEDICATED TO THE I/O
- SPECIAL FEEDTHROUGH PATHS
- ARITHMETIC PROCESSING CAN OCCUR AT THE SAME TIME AS I/O TRANSFERS
- ALL PORTS CAN BE USED IN ANY CLOCK CYCLE AND AT ANY RATE

REGISTER FILE ARCHITECTURE

[Diagram showing the register file architecture with ports and paths labeled.

6.14]
GATE ARRAY

- Netlist is designed using the customer's expertise
- Designed in a gate array environment
- Library contains over 200 cells
- Propagation delays are typically 0.5 ns per gate
- Full static CMOS gates
- Low power consumption
- Designs of 30k gates are possible
- Variable aspect ratio and shape

0.8 μm DLM CMOS Process

Metal 1 Pitch: 2.0 μm (No Contacts)  
               2.6 μm (With Contacts)

Metal 2 Pitch: 2.0 μm (No Vias)  
               2.6 μm (With Vias)

Drawn Poly Width: 0.8 μm

Poly Space: 1.0 μm (Over Field)  
            1.5 μm (Over Diffusion)

Contact Size: 0.8 X 0.8 μm**2

Via Size: 0.8 X 0.8 μm**2
0.8 um DLM CMOS ELECTRICAL PARAMETERS

Leff, p = 0.7 um  Leff, n = 0.6 um

SILICIDED POLY RESISTANCE: 2.0 ohms / sq
SILICIDED DIFFUSION RESISTANCE: 2.0 ohms / sq

REFERENCE:
CHAPMAN, RICHARD A., "AN 0.8 UM CMOS TECHNOLOGY FOR HIGH PERFORMANCE LOGIC APPLICATIONS", IEDM 1987.

FIRST IMPLEMENTATION

- COPROCESSOR FOR A PA–RISC PROCESSOR USED IN HP'S SERIES 700 WORKSTATION FAMILY
- MEGACELL'S FLEXIBILITY MEET CUSTOMER'S REQUIREMENTS
  FREQUENCY
  ARCHITECTURE
  LATENCY (3 CYCLE)
  THROUGHPUT (2 CYCLE)
- ADDITIONAL INSTRUCTIONS WERE ADDED TO MAXIMIZE PERFORMANCE
  3–REGISTER MULTIPLY
  INDEPENDENT 2 REGISTER ADD OR SUBTRACT
  ACCELERATED CLIP TEST
  RECIPROCAL SQUARE ROOT
  INTEGER MULTIPLY
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FIRST IMPLEMENTATION RESULTS:

DIE SIZE: 502 X 518 MILS
TRANSISTOR COUNT: 640K
PACKAGE: 207 PIN CERAMIC PGA
POWER: 5.0 WATS AT 66 MHZ
SPEED: 66 MHZ, WORST CASE CONDITIONS

LINPACK BENCHMARK (100 X 100)
SINGLE PRECISION: 33.2 MFLOPS
DOUBLE PRECISION: 23.0 MFLOPS

<table>
<thead>
<tr>
<th>Architecture</th>
<th>PA-RISC</th>
<th>PA-RISC</th>
<th>RS/6000</th>
<th>SPARC</th>
<th>MIPS</th>
<th>68000</th>
<th>68040</th>
<th>486</th>
<th>i860</th>
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<td>33</td>
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<tr>
<td></td>
<td>espresso</td>
<td>42.5</td>
<td>55.2</td>
<td>24.9</td>
<td>19.0</td>
<td>26.3</td>
<td>23.0</td>
<td>13.4</td>
<td>17.1</td>
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<td></td>
<td>li</td>
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<td></td>
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</table>

Table 1. SPEC benchmark results. These represent the highest clock rates currently available in systems, except for IBM's 41.6-
MHz RS/6000 Model 550 which was excluded because it is not in the same price class. Note PA results are for June '91 compiler
release. The systems are the HP 9000 Model 720; HP 9000 Model 730; IBM RS/6000 Model 540; Sun SPARCstation 2; MIPS
RC3360; Motorola Delta Series Model 8512; HP 425s; and Alacron AL860. All machines except i860 have external cache.
SUMMARY

- QUICK TIME-TO-MARKET
- HIGH PERFORMANCE
- FLEXIBLE ARCHITECTURE
- MEGACELL SOLUTION WORKS AT 66 MHZ IN UNIX SYSTEM
- FUNCTIONAL ON FIRST SILICON