82495DX/82490DX
A HIGH PERFORMANCE 2ND LEVEL CACHE
FOR THE Intel486™ DX CPU

ADI GOLBERT
INTEL ISRAEL

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AGENDA

- System Model
- Objectives
- The Product
- Architecture
- Performance
- Conclusions
SYSTEM MODEL

CPU BUS
LIFE SPAN
6-18 MON.

MEMORY BUS
LIFE SPAN
2-3 YEARS

STANDARD BUS
LIFE SPAN
5-10 YEARS

CPU

CACHE
MEM. BUS
INTERFACE

MEMORY

DNA AND
COPROCESSORS

- Highest performance
- Fastest Clock
- High Bandwidth
- Short Life Span

- High Performance
- Multiple Protocols
- Differentiation
- Medium Life Span

- Standardization
- Compatible Products
- Preserve Investment
- Lower Performance
- Long Life Span

82495DX/490DX CACHE OBJECTIVES

- Deliver High Performance
  - 50 Mhz, Zero Wait-State RDs/WRs
  - Concurrent CPU/MEM Bus Transactions
  - Large Cache Size (upto 512Kbytes)
  - Two-Way Set Associative

- Simplify Multi-Processing Designs
  - Hardware Cache Consistency

- High Integration
  - Minimum Number of Devices

- Provide Flexible Memory Bus Interface
  - User Differentiated
  - Synchronous / Asynchronous

- Software Transparent
THE PRODUCT

MARKET: HIGH-END DESKTOPS / SERVERS

Intel486™ DX 50Mhz CPU-Cache Module

Intel®

82495DX/490DX CACHE FEATURES

- Two Chip Set
  - Controller (82495DX)
  - Dual Ported Intelligent SRAM (82490DX)

- Cache Sizes: 128, 256, 512 Kbytes

- 0-WS Support for 50 Mhz Intel486™ DX CPU

- Multi-Processing Support
  - Write-Back Snoopy Cache, MESI-Consistency
  - 2-way Set Associative,
    Most-Recently-Used (MRU) Way Prediction
  - Multi-level Consistency Through Inclusion

- Flexible Memory Bus Interface
  - Synchronous / Asynchronous, 32/64/128 Bits

- Available as Components / CPU-Cache Module
CPU / CACHE CORE

Intel486 DX CPU

82495DX Cache Controller

82490DX Dual Ported Intelligent SRAM (256 Kbits) (4x to 16x Devices)

Memory Bus Controller

• Integrated Tags and Cache Control
• Cache Consistency
  - MESI on Memory Bus
  - Inclusion on CPU Bus
• Two Way Associative
  - MRU Prediction / Correction
  - In Lock-step with 82490DX
• Innovative / Flexible MBC Interface
  - 4 / 8 Transaction Burst
  - Sync / Async Snoops
  - With / Without Write-Allocation
  - Pipelined
MULTIPROCESSING FEATURES

- Hardware-Based MESI Consistency Protocol
- Allocate On Write To Minimize Bus Traffic
- High Bus Snoop Rates
- Cache To Cache Data Transfers
- Asynchronous System Bus Operation
- Consistency With CPU-L1-Cache by Inclusion

CACHE HIGHLIGHTS

82490DX - DUAL PORTED INTELLIGENT SRAM

- 2-WAY SRAM ARRAY (256 Kbits)
  - MRU Prediction
- Line Wide Buffers (upto 128Bytes)
  - Write-Throughs, Line-Fill
  - Write-Back (2), Snoop
  - One CLK Array Access
- Dual Ported
  - CPU / MEM Bus concurrency
- Line-Size: 16 / 32 / 64 / 128 Bytes
- MEM-BUS: 32 / 64 / 128 Bits Wide
- SYNC / ASYNC Interface
MRU-WAY-PREDICTION

495DX

WAY 0

490DX

WAY 0

WAY 1

DATA OUT

PREDICTION CORRECTION

WAY

1st BHDY

TUNED CPU/CACHE INTERFACE

50 MHZ, 2-WAY, 0-WAIT-STATE

CPU

CACHE CONTROL

CYC QUALIFIER

GROUP 1

DUAL PORTED INTELLIGENT SRAM

MSS DOMAIN

OPTIMIZED FOR MODULES
PERFORMANCE
IMPROVEMENT VS 25 MHZ STAND-ALONE Intel486™ DX
SPEC 1.0 BENCHMARK

BUS: @ 25 Mhz, PH=2WS, PM=5WS, BURST=1,2,1

BUS UTILIZATION
Average Of 9 Program Traces: 6 Unix, 3 DOS
Data From Performance Simulations

Fast Bus: Ph=1WS, Pm=4WS, Burst=1,1,1
Slow Bus: Ph=4WS, Pm=10WS, Burst=2,2,2
CONCLUSIONS

• A High Performance Cache For The Intel486™ DX Was Presented

• It Offers
  - High Integration
    Cache Controller, Dual-Ported-Intelligent-SRAM
  - High Performance
    50 Mhz, 2-Way-Cache, 0-WS
    TUNED CPU BUS
    MODULE READY
  - Multi-Processing
    Write-Back
    MESI Cache Consistency