Typical system design has high theoretical bandwidth, limited by protocols, decoding, muxing, ECC, etc. Effective bus usage is 50% with up to 75% with deep interleaving. Might get 2 read accesses out of DRAM any 20ns.

For us, less attention (but still substantial) should be on MPSoC's DRAM, but RASX requirements (e.g., cache fill) saturate many bus.

PROBLEMS 1. Access times should be lower
- Bandwidth of AOM isn't high enough
- Wider DRAM desirable for low cost systems
- RAM space should be tightened.

RAMBUS 512Kx9 is 14% larger than normal RAM. @16Mb = 16%
64Mb = 5%

RAMBUS controller with RAM of 12Ms
FTP via hplsci.hpl.hp.com

MPS/68K CPUAM: try to improve latency & bandwidth by changing or
VLIW adder 66ns to 40x40 DRAM. CAN THIS BE
ONCE WITH DRAM OR DOES INCREASE PROBLEM-
DIMINUTIVE THIS?

II symmetrical DRAM. Normal DRAM with input & output.

RAMBUS access is ~150-200NS now because they do a flush before the access. For size is
~100NS. RAMBUS seems to be much faster.

CAN ATTEMPT ALL ONCE METHOD. MY BE SLOWER
WITH RASX TO INCREASE PERFORMANCE.