Alpha Architecture
and
DECchip 21064

Presentation Outline

Alpha Architecture
  Goals
  Overview
  Features
DECchip 21064
  Facts
  Overview
  Features
  Interface
Alpha Architecture Goals

Performance - Longevity - Scalability - Generality

Multiple issue (bottlenecks removed)
Operating System Independance (VMS, OSF/1, NT)
64 bit Data and Address Space (linear)
Multiprocessor support
Efficient support for multiple languages
Binary migration of software (VAX and MIPS on day one)

Architecture Overview

General
64 bit Load/Store machine
32 bit fixed length instructions

Data Types
8b, 16b, 32b, and 64b integers
VAX 32b and 64b floating point formats
IEEE 32b and 64b floating point formats

Support for MP
Hardware synchronization primitive (ldx_l/stx_c)
Read/Write ordering & memory barrier
Processor number (whami) and per processor 64b value/ptr (sysval)
Architecture Overview cont.

32 - 64 bit integer registers (r0..r31)
   r30 used as stack pointer (sp)
   r31 hardwired as zero
32 - 64 bit floating point registers (fr0..fr31)
   fr31 hardwired as zero
64 bit program counter (pc)
32 bit cycle counter (pcc)
FPCSR - 7 status bits, 2 rounding control bits
64 bit virtual addresses (64 bits checked; subsets implemented)
64 bit thread unique register

Instruction Formats

```
Call_Pal
  3 22 22 0 0
  1 65 65 10 65

BR
  3 22 22 11 0
  1 65 10 65 0

MEM
  3 22 22 11 0 0 0
  1 65 10 65 54 0

OP
  3 22 22 11 func 0
  1 65 10 65 54 0
```
Alpha Features

Avoid Implementation Bottlenecks
No CC's, Side effects, Mode bits, Byte writes
Conditional Move Instructions (Integer and FP)
Large relative branch range (+/- 4Mbytes)
Exclude potential "First implementation artifacts’
  Branch delays, Load delays

Alpha Features

Encourage Hardware/Software teamwork

MB, TRAPB Instructions
  Identify critical interactions

HINTs improve
  TB utilization (4 Granularity sizes)
  Fetcher efficency (Absolute jump, Subroutines, Branch)
  Software prefetching (FETCH instruction)
Privileged Architecture Library

Provides optional insulation from hardware details for Operating Systems and applications

Privileged Mode

- Physical I/O stream
- Interrupts disabled

Special Instructions

- Access all internal state
  - Private GPRs
- Virtual or Physical LD/ST
- Privileged jump

Strict Coding Rules

- Software timing

Applications

Operating System

PAL

HW

DECchip 21064

The First Alpha Implementation
## Chip Facts

<table>
<thead>
<tr>
<th>Specification</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycle time</td>
<td>6.6nS (150MHz) / 5.0 nS (200MHz)</td>
</tr>
<tr>
<td>Process technology</td>
<td>CMOS-4 (0.75μm), 0.5μm Leff, 3 metal layers</td>
</tr>
<tr>
<td>Die Size</td>
<td>13.9mm X 16.8mm</td>
</tr>
<tr>
<td>Transistor count</td>
<td>1.68 million</td>
</tr>
<tr>
<td>Package</td>
<td>431 pin PGA (291 signals)</td>
</tr>
<tr>
<td>Power dissipation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>30W Typical @ 200MHz (3.3V Vdd)</td>
</tr>
<tr>
<td></td>
<td>23W Typical @ 150MHz (3.3V Vdd)</td>
</tr>
</tbody>
</table>

## Chip Facts cont.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtual address size</td>
<td>$2^{43}$ byte addresses (linear)</td>
</tr>
<tr>
<td>Phys address size</td>
<td>$2^{34}$ byte addresses</td>
</tr>
<tr>
<td>Issue rate</td>
<td>Two instructions per CPU cycle</td>
</tr>
<tr>
<td>Functional units</td>
<td>Integer Op, FP Op, Ld/St, Branch</td>
</tr>
<tr>
<td>Translation buffers</td>
<td>32 data, 12 instruction (fully associative)</td>
</tr>
<tr>
<td>Write buffer</td>
<td>4 entries X 32 bytes/entry</td>
</tr>
<tr>
<td>Primary caches</td>
<td>8kB Icache, 8kB Dcache (direct mapped)</td>
</tr>
<tr>
<td>Bus interface</td>
<td>128/64b data + 34b address</td>
</tr>
</tbody>
</table>
Single Wire Clock

Data In
CLK
Vdd
Vdd
Vdd
Vdd

A Latch
B Latch

Data Out

Chip Block Diagram

ICACHE
EBOX
IBOX
FRF
FBOX
IRF
ABOX
Write Buffer
DCACHE
BIU
Dual Issue

Choose Two:
- Integer Operate (IOP)
- Floating Point Operate (FOP)
- Branch (FPBR, IBR)
- Load/Store (ILD, FPLD, IST, FPST)

ALL Pairs Dual Issue except
IOP -- FPBR, FPST
FOP -- IBR, IST

Chip Features

I-stream support
- Stream Buffer prefetches in-line code
- Branch History Table / JSR Stack / Bubble Squash
- Translation Buffer range >16Mbytes plus Super page

D-stream support
- Pending Load / Wrapped Reads improve latency
- Burst mode RAM support, first/remaining access times
- Hit under Miss
- Pending Store, fully pipeline load/stores to cache
- Translation Buffer range 128Mbytes plus Super page
Code Tuning

RPCC Instruction
- Fine Grain and Process Virtual Times

Performance Counters on Chip
- Generate PC Histograms
- Instruction Issue Characteristics
  Issue / Stall / Instruction Type
- On Chip Cache Performance
- Two System Input Pins
  Bcache, External Transactions

Interface Goals

Interface to Industry Standard Components
Scalable System Designs
- Flexible Bcache Size and Speed
- Flexible System Interface Speed
- Without Scaling CPU Speed
Usable Test Features
Pin Bus Features

Balance Performance / Flexibility / Simplicity
- BCache Sizes from 128KB -> 16MB (or none)
- BCache Latencies from 3 to 16 CPU cycles
- 128 or 64-bit Data Bus, chosen at reset
- System Interface clock from 1/2 to 1/8 CPU clock
  No 200MHz System Logic
- Cache Policy flexible, left to system designer
- TTL or ECL levels
- Longword ECC or Parity
- Simple Diagnostic Interface to off-chip Serial ROM
Data Bandwidth

<table>
<thead>
<tr>
<th></th>
<th>200 MHz</th>
<th>150 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Icache/Dcache</td>
<td>1.6 Gbyte/s</td>
<td>1.2 Gbyte/s</td>
</tr>
<tr>
<td>Bcache</td>
<td>1.28 Gbyte/s</td>
<td>0.96 Gbyte/s</td>
</tr>
<tr>
<td>Memory Write (no Bcache)</td>
<td>0.8 Gbyte/s</td>
<td>0.6 Gbytes/s</td>
</tr>
<tr>
<td>Memory Read</td>
<td>System limited</td>
<td></td>
</tr>
</tbody>
</table>

Conclusion

Alpha Architecture
- Facilitates High Performance Designs
- Operating System Independant
- Long Term Growth

DECchip 21064
- Performance Unmatched (400 MIPS, 200MFLOPs peak)
- Widely Scalable Interface
- First of Family
- 150 MHz Available Today