Multiprocessor Features of a PA-RISC Processor Interface Chip

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• Introduction
• System Organization
• Multiprocessor Features
• Performance Results
• Summary
Design Goals

- General Purpose Multiuser System
  Technical and Commercial Applications

- Scalable Performance
  Uniprocessor to > 8-way Multiprocessor

- Platform for Multiple Generations of Systems
  Independent Upgrades of Processor,
  Memory and I/O

Design Approach

- Processor
  High integer and FP throughput
  Large first-level external cache

- Memory
  Large physical memory
  Highly interleaved

- I/O
  High connectivity to mass storage
  High bandwidth bus adapter

- Bus
  Low latency
  High bandwidth
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DO mln DATA RETURN, EACH SPOUTING
TO OCCUR AT THE SAME TIME?

IS DIARY HAVE MANY 2X MB ACCESS?

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**System Organization**

- Processor
- Processor
- Memory Array
- Memory Array
- Processor Memory Bus (480/960 MB/s)
- Service/Control Processor
- Dual Bus Adapter
- Dual Bus Adapter
- HP-PB
- HP-PB
- 14 I/O Slots
- 14 I/O Slots
- HP-PB
- HP-PB
- HP-PB
- HP-PB

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Bus Specifications

- 16-slot backplane
- 60-MHz worst case frequency
- 960 or 480 megabyte/second bandwidth
- 128-bit or 64-bit data bus
- Separate data and address paths
- Data protected with ECC, address with parity

Synchronous Pipelined Bus
**Bandwidth Enhancement Features**

- Flexible memory interleaving
  - Up to 64-way interleaving for each of 3 groups
  - Unified memory interleaving among non power of 2 modules
- Resource-driven arbitration
  - Memory block status maintained by masters
  - Transactions not queued by memory
- Slave-driven arbitration
  - I/O re-arbitrates when data available

**Cache Coherence Transaction**

- Bus protocol for cache and TLB coherence
- Processor-to-processor data transfer

![Diagram of cache coherence transaction](image)

- Address Bus:
  - Coherent Read
  - 3rd Party Signals Hit
  - Proc to Proc Transfer

- Data Bus:
  - Memory Data
  - 3rd Party Data

- Master Processor
- 3rd Party Processor
- Memory
Cache Coherence (cont’d)

- Snoopy cache coherence with duplicate cache tags
- Multiple outstanding coherence checks

![Diagram of cache coherence]

Write Buffers

- Circular FIFO with random access

![Diagram of write buffers]
Multiprocessor Tuning Features

- Configurable bus parameters
  Memory latency and cycle time
  Coherence check
  Interleave factor
- Pipeline freeze capability
  Coherence exception conditions
- Performance monitoring counters
  Multiprocessor events
- Support multiple generations of CPUs
  
  die photograph

3.35 x 16 mm (1/8 x 5/32 in)
60 MHz QEM57
PGA (missing S128)
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TPCA - 578 TPS (4-way) 60M2CPI 60MIPS 1685
SPEE RATE 1174 2360 3529 4685
FP 92 (1.0) (2.01) (3.0) (3.99)
SPEE RATE 1164 2253 3306 4301
INT 92 (1.0) (1.0) (2.84) (3.70)

Performance Results

This slide will present UP and MP performance results.
Summary

Demonstrated a highly scalable many-way MP system using high performance RISC CPUs

Achieved 8-way MP with first silicon

Draw gc or 9

2.1.10