On-chip cache hierarchy for 1000-MIPS multi-superscalar processor

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Objective of this work

To achieve a maximum processor performance on a single chip using 0.3 μm BiCMOS technology
Microprocessor performance and its prediction

Year

Performance (MIPS)

250MHz (0.3μm)

clock 70-100MHz

HotChips IV

Integration capacity using 0.3μm BiCMOS

<table>
<thead>
<tr>
<th></th>
<th>performance</th>
<th>area</th>
<th>capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Superscalar RISC</td>
<td>clock cycle 3.1 ns</td>
<td>6.6mm²/RISC</td>
<td>4 RISCs</td>
</tr>
<tr>
<td>FPU</td>
<td>3.5 ns (53bX27b Mult.+Adder)</td>
<td>9.1mm²/FPU</td>
<td>4 FPUs</td>
</tr>
<tr>
<td>Cache memory</td>
<td>2.8 ns</td>
<td>60mm²/128KB</td>
<td>max 256KB</td>
</tr>
</tbody>
</table>
High performance single chip strategies

(1) Uni-processor

0.3 μm BiCMOS technology
Dual ALU superscalar architecture

(2) Multi-processor

Interleaved shared cache memory

Two on-chip cache strategies

One-level

Large private caches

Two-level

Small private caches and 4-way interleaved secondary cache
Split-bus with 4-way interleaved secondary cache

Access reduction by private caches

- Average Interval: 1.83 → 4.51
- Peak traffic → $\frac{1}{3}$

- Without caches
- With 1KB caches

External Access Intervals

Clocks
Simulation models

(1) Interlock bus without SC
(2) Interlock bus with SC
(3) Split bus with Interleaved SC

Simulation results of three on-chip cache models

HotChipsIV
Photomicrograph of experimental chip

8.0 x 8.1mm
0.3 μm BiCMOS
1.02 MTrs.
(Bip. 20 KTrs.)

QC-BiCMOS circuit and delay time

3-NAND (FO=5)

BICMOS
(Conventional)
CMOS
QC-BiCMOS

Delay time (ps)

QC-BiCMOS circuit

nnp
Quasi-pnp
pnk

HotChipsIV
Cache / TLB tag comparator

**HotChipsIV**

Critical path delays

Vcc = 3.3 V, T = 20 C
Conclusion

A 250MHz, 1000MIPS multi-superscalar processor using QC-BiCMOS

Featuring
- On-chip interleaved secondary cache memory
- ECL-sense amplifier merged comparator and selectors