The Project

- Highly Integrated SPARC processor
- SPARC V8 32-bit architecture
- Processor targeted for low cost systems
- The first of a series
- Reusable design core
Tsunami Functionality

- SPARC V8 Integer Unit
- IEEE 754 Floating Point Unit
  FPU core licenced from Meiko Ltd, UK
- SPARC reference MMU
- SUN-4M IOMMU
- 4K Instruction Cache, 2K Data Cache
- Memory controller (direct DRAM interface)
- Sbus controller (Sbus rev A.2 compatible)
- IEEE 1149.1 JTAG controller and clock controller
- 288 Pin TAB Package
The Challenge

- Short time-to-**volume** - 10^3 of MOS is as quickly as possible
- Low manufacturing cost
- High level of functional integration on-chip
- Integrate into existing multi-vendor CAD environment
  - Unix, Verilog **HDL**, SynOpSys **synthesis**, Motive **Timing Analyzer**
- **Full Custom Performance in ASIC Design Cycles**
- Utilize Existing Expertise
  - ASIC designers, Computer architects, few physical designers

The Solutions

- **Short time-to-volume**
  - Requires "correct-by-construction" design methodology
  - First Silicon must meet spec
  - Leverage Heavily

- **Low cost**
  - Use mature Silicon technology
  - Selected TI's .8micron, 2 layer metal, mainstream process
  - TAB packaging

- **High level of integration**
  - "Custom" style density required
  - Datapath Automation

- **Use existing staff; primarily ASIC design experience**
  - Use logical & physical synthesis to de-skill custom IC design

- **Integrate into existing multi-vendor CAD environment**
  - Open interfaces,
  - Unix level access to database
Overall Approach

- High Leverage
- Simple Efficient Pipeline
- High level of Testability/Debugability
- Vertical Design Engineers
- Conservative Circuit Design
- Largely automated CAD flow
  Selected Silicon Compiler toolset (GDT) from Mentor Graphics

Leverage Areas

- Partnership with Si Vendor (Texas Instruments)
  Std. Cell Library in GDT
  Expertise in RAM array design
  Expertise in GDT tools

- Sun existing designs:
  Utilized a debugged 5-stage IU pipeline
  Large suite of diagnostics and tests from other projects

- Licensed the Floating Point Core from Meiko Ltd.
  Fully verified IEEE compliant design with verification suite

- Partnership with Mentor Graphics
  Design of speed critical "generator" based sections
Testability, Clock & JTAG

- IEEE 1149.1 JTAG compliance including boundary scan.
- Core is on one single scan loop (about 3500 FFs)
  ATPG has been run on Tsunami with 90+% fault coverage
- Clock control allows precise clock-stop and single-stepping.
  Tsunami is the source for system & Sbus clocks - Simplifies system design
  Two level clock buffering with well matched skews
  Used selected events as triggers to stop clocks during system debug
- Nondestructive Scan.
  Enabled dump-modify-restore operations in systems and on testers
- Utilized scan for timing debug on testers
  Stretch cycles selectively to identify failing cycles.
  Dump scan chain to view affected FFs and compare with simulations to identify failing long paths.

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CAD Approach

- "Tall-Thin" Vertical Design Engineers.
  - Vertical Responsibilities:
    Verilog RTL
    Synopsys
    Unit-level Verification
    Timing analysis (pre and post layout)
    Megacell Functional and timing Specs
    Unit-level layout
    Scan connectivity and verification
    Unit-level switch-simulation
    Unit-level Physical Design Verification (DRC, LVS)
  - Global Group did megacells, IOs, chip-composition and verification

- Compiled Custom Design:
  - A few timing/area critical blocks/cells done as hand-optimized custom
    e.g. RAMs, TLB, Reg Files, ROM, Std. Cells, Fast ALUs etc.
  - Some regular structures designed using Data Path Compilers
    Provide reasonable density, flexibility to changes, timing remains stable
  - Most control logic layout used Auto place and route tools.
    Provided 100% route completion, fully DRC and LVS clean
The Design Flow

- Verilog RTL
- FloorPlanning
- Megacell Blocks
- DataPath Blocks
- Control Blocks
- Chip Integration
- Test Tape
- Mask Tape

CAD Approach (contd...)

- Databases:
  - Central Databases with SCCS revision control
  - Access from two coasts, since the design team was in Mtn. View and Boston.
  - All tools centralized
  - Unified CAD and network environments for all designers

- Automation:
  - Push button flow for SPR (Std. Cell Place and Route) and DPR (Data Path Route)
  - Automatic post-placement scan chain stitching
  - Automatic post-placement Clock buffer insertion
  - Leaf cells laid out in GDT, automatically characterized and verified using a flow called "autochar".

- AutoChar flow for Libraries:
  - Ran HSPICE characterization on all leaf cells. Provided timing data.
  - Generated a cell database called CDB.
  - CDB provided a consistent source for other library views
CAD Approach (Contd...)

- **Timing:**
  - Initial constraints provided to Synopsys. Wireload models used.
  - Block level route parasitics extracted to get block level timing.
  - Chip route parasitics extracted to get overall timing.
  - Resistive and cross-coupling effects of long wires included.

- **Closing the Loop:**
  - Instruction-by-instruction comparison of simulations with SPARCSim (Sparc Architectural Simulator)
  - Full-chip post-layout extracted gate-level Verilog regression
  - Full-chip backannotated timing

- **Management:**
  - Unified task-tracking database provided a mechanism to tie in weekly individual status reporting with schedule updating and tracking.
Resources

- **Manpower:**
  - 25 engineers at Sun including both coasts (peak was higher)
  - Only two mask designers needed
- **Tools & vendor selection to tapeout was 15 months. Silicon 18 months**
- **Machines:**
  - Verification of the RTL design took the most resources
  - About 80 Sun servers of the 4/470 class were used for simulations/ regressions/vector-extraction
  - About 15 machines of the same class were used for Physical Design validation and LSIM regressions.
- **Licenses:**
  - Site Licenses for Verilog, Synopsys and Motive licenses.
  - 15 GDT licenses, 4 Checkmate licenses, 4 Compose licenses.

  Most licenses were floating ones

TSUNAMI SPARC PROCESSOR
Sun Microsystems Inc.

What We Learned

- **Turnaround times:**
  - Quick iterations from RTL to Layout to RTL are key
    - Enable early design decisions.
- **Automation:**
  - Automated flow is a good choice when you can compromise on area but not on schedule
- **CAD Tools:**
  - Tool openness is crucial. Ability to choose the best point tools is vital.
  - Close interaction with the vendor is important when pushing the envelope.
- **Design Environment:**
  - Central databases, revision control and unified environments are essential while managing large/multi-coastal teams.