GaAs VLSI Enhancement through the Utilization of Global Optical Free Space "Smart" Interconnects

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Logic Family Comparison

\[ \triangle = \text{TTL} \quad \bigcirc = \text{CMOS} \quad \bigcirc = \text{ECL} \quad \square = \text{GaAs} \]

Power Consumption

Switching Speed

100mW

100pJ

10pJ

1pJ

1mW

GaAs/ecl

1ns

10ns

5400

@ 20Mhz

@ 5Mhz

@ 1Mhz

5000

@ 5Mhz

@ 1Mhz

7.2.1
Digital photonic and electrical switching energies
(Power Dissipation vs. Switching Time)

"Smart" Interconnect

\[ \overline{a_1} + \overline{a_2} + \overline{a_3} + \ldots + \overline{a_N} = a_1 a_2 a_3 \ldots a_N \]
## Detection Negation Amplification Emission (DANE) Specifications

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of DANE cells</td>
<td>32 x 32</td>
</tr>
<tr>
<td>Optical gain</td>
<td>1,000</td>
</tr>
<tr>
<td>Electrical gain</td>
<td>10,000</td>
</tr>
<tr>
<td>Max fan-out</td>
<td>128</td>
</tr>
<tr>
<td>Threshold (detection)</td>
<td>-37dbm @ $10^{-18}$ BER or 0.2μW</td>
</tr>
<tr>
<td>Switching energy</td>
<td>&lt; 1.2fJ</td>
</tr>
<tr>
<td>Gain characteristic</td>
<td>Limiting 1-bit</td>
</tr>
<tr>
<td>Min SNR (after fan-in)</td>
<td>13db</td>
</tr>
<tr>
<td>Min. optical output power/cell</td>
<td>0.2mW</td>
</tr>
<tr>
<td>Max power dissipation/cell</td>
<td>1W/cm²</td>
</tr>
<tr>
<td>Max one cell size</td>
<td>0.1mm²</td>
</tr>
<tr>
<td>Laser modulation</td>
<td>RTZ</td>
</tr>
<tr>
<td>Data rate</td>
<td>&gt;400 MHz</td>
</tr>
</tbody>
</table>

## 2D DANE Subsystem

![2D DANE Subsystem Diagram](image)

- 2-D VCSEL array
- Optical input plane
- Optical output plane
- Silicon carrier
- 2-D detector and FET circuit array
- Edge connector
2 D single stage global free space interconnect minterm formulation.

Global Freespace Interconnect realization for matrix tensor

2D Array of holograms with fixed interconnects

2D Array of Surface Emitting Laser Diodes

Amplification & Negation
Detection (-V) Emission (gad)

DANE output produces minterms for realization of matrix tensor logic

one DANE cell

Cross-section of the 2-D DANE subsystem

Photodetector and FET circuit array
Solder bump
Via hole
Anti-reflection coating
1 DANE pixel
Optical input plane
Optical output plane
GaAs substrate
Edge connector

Heat sink

7.2.4
Cross-section of a silicon carrier showing cooling channels and via holes

Integration of GaAs Detectors with HEMTs
2D multi-stage global free space interconnect processing

2D Array of holograms with fixed interconnects

"AND" Interconnects

Formulation of minterms

2D Array of holograms with fixed interconnects

"OR" Interconnects

Forming arbitrary switching functions through holographic optical elements providing full global interconnects

Smart Pixel + N^5

Smart Pixel - DANE cell

Metal Semiconductor Metal GaAs detector

HEMT/MESFET Gain/Inversion

Single quantum well laser diode

Detection, Amplification, Negation, and Emission

Logic detection and signal conditioning area

Distributed Bragg Reflection (DBR) diode region for wavelength selection

\[ \sum_{i=1}^{N} a_i \]

Interconnect selection

Apply DeMorgan's theorem

\[ = a_1 a_2 a_3 \ldots a_N \]
DANE/DBR N^5 Global Interconnect Modules
"Smart" Holographic Interconnect for a 3:8 Decoder

Optical Multichip Modules
"Smart" chip-to-chip level interconnects with optical bus and address decode
Addition - $\tau = 1\Delta T$ (one clock/cycle)

Addition - (one clock) Optical Free Space Global Interconnect Primitive Implementation.

$$A = A_{n-1} A_{n-2} \ldots A_1 A_0 \quad A_{n-1} B_{n-1} \quad \text{Most Significant Bit (MSB)}$$

$$B = B_{n-1} B_{n-2} \ldots B_1 B_0 \quad A_0 B_0 \quad \text{Least Significant Bit (LSB)}$$

Step 1 - Calculate partial sum and partial carry (asynchronous, electronic)

$$P_k = A_k \oplus B_k \quad G_k = A_k \cdot B_k$$

Step 2 - Calculate true look ahead carry (synchronous, optical)

$$C_m = G_m + \sum_{i=1}^{m} G_{m-i} \prod_{j=1}^{i} P_{m+i-j}$$

Step 3 - Calculate true summation (synchronous, electronic)

$$S_m = P_m \oplus C_{m-1}$$
Addition - Partial carry for 5 bit addition:

\[ C_{i1} = G_0 \quad C_{i2} = 0 \quad C_{i3} = 0 \quad C_{i4} = 0 \quad C_{i5} = 0 \]
\[ C_{21} = G_1 \quad C_{22} = G_0 P_1 \quad C_{23} = 0 \quad C_{24} = 0 \quad C_{25} = 0 \]
\[ C_{31} = G_2 \quad C_{32} = G_1 P_2 \quad C_{33} = G_0 P_1 P_2 \quad C_{34} = 0 \quad C_{35} = 0 \]
\[ C_{41} = G_3 \quad C_{42} = G_2 P_3 \quad C_{43} = G_1 P_2 P_3 \quad C_{44} = G_0 P_1 P_2 P_3 \quad C_{45} = 0 \]
\[ C_{51} = G_4 \quad C_{52} = G_3 P_4 \quad C_{53} = G_2 P_3 P_4 \quad C_{54} = G_1 P_2 P_3 P_4 \quad C_{55} = G_0 P_1 P_2 P_3 P_4 \]

True carry \[ C_1 = \sum_k C_{ik} \]

Total number of interconnects for lookahead carry \[ 9 \times 5^2 = 225 \]

Total number of active interconnects for lookahead carry \[ 9 \times 15 = 135 \]

Addition - Optical Free Space Global Interconnect Primitive Implementation.

\[ C_m = G_m + \sum_{i=1}^{m} G_{m-i} \prod_{j=i}^{i+j} P_{m+i-j} \]

General Expression:

\[ C_0 = G_0 \]
\[ C_1 = G_1 + G_0 P \]
\[ C_2 = G_2 + G_1 P_2 + G_0 P_1 P_2 \]
\[ C_3 = G_3 + G_2 P_3 + G_1 P_2 P_3 + G_0 P_1 P_2 P_3 \]
\[ \vdots \]
\[ C_i = G_i + G_{i-1} P_{i-1} + G_{i-2} P_{i-2} \ldots + G_0 P_1 \ldots P_{i-1} \]
\[ C_{i+1} = G_{i+1} + G_i P_{i+1} + G_{i-1} P_{i+1} \ldots + G_0 P_1 \ldots P_{i+1} \]
Addition
Example for 5bit addition

Processing (Inversion, OR-ing) Photodiode matrix

Addition
Example for 64 bit addition

Detection and Processing Plane
Providing true carry in each digit.

Photodiode matrix
Summary

Primary Benefits

- Low Power
- Low BER ($<10^{-18}$)
- Smart pixels (high fan-in and fan-out)
- High algorithmic efficiency through increased fan-in

Secondary Benefits

- No capacitive loading: fan-in limited only by contrast ratio
- No signal dispersion
- No signal skew
- No cross talk between channels