hyperSPARC™ Modules: AKA PINACLE.

The Second Generation SPARCore™ MBus Modules

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Program Objectives

- Performance
  - 2–4X current generation SPARCore MBus modules
  - 55.5 – 100 MHz + clock frequencies

- Compatibility
  - 100% SPARC Architecture (Version 8) compliant
  - SPARC Reference MMU
  - SPARC MBus (Level 2)

- Upgradeability
  - 100% hardware compatible with current MBus modules

- Manufacturability
  - Simple, proven CMOS process technology
**hyperSPARC System Configuration**

- CY7C620 CPU
- Intra-Module Bus (32-bit address/64-bit data non-multiplexed bus)
- CY7C625 CMTU
- CY7C627 CDU
- 128-Kbytes
- 256-Kbytes (OPTIONAL)
- Synchronous SRAMs
- SPARC MBus (64-bit multiplexed address/data bus)

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**CY7C620 Central Processor Unit**

- Combined IU, FPU, and I-cache
- Superscalar
- Dual instruction fetch, launch, and execute
- Balanced, highly-pipelined microarchitecture
- 1-clock primary cache miss penalty
- 1.5M transistors
**CY7C620 Execution Units**

Unrestricted, Unaligned Dual Launch:

- **Integer Unit**
  - 32-bit pipelined (5-stage) ALU

- **Load/Store Unit**
  - 64-bit data path, independent of integer ALU

- **Floating Point Unit**
  - 64-bit pipelined (5-stage) multiplier
  - 64-bit pipelined (5-stage) adder

- **Branch/Call Unit**

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**CY7C620 Block Diagram**
**CY7C620 FP Queue**

**CY7C620 Fast Constant/Index**

Fast constant:

```
set 0Xfe11c12, %g1
```

```
sethi (hi imm), %g1
or %g1, (lo imm), %g1
```

CY7C620 executes these two as if they were one instruction

Fast index:

```
sethi
ld
```
CY7C620 Fast Branch

- Allows conditional branch and associated ALU instruction to be launched simultaneously
- Instruction throughput increased
  - Branch taken, target fetched 1 cycle sooner
  - Branch not taken, instruction stream resumed 1 cycle sooner

CY7C625 Cache Controller, MMU, & Tag Unit

- Combined cache controller, MMU
- Supports 128K or 256K virtual cache
- Dual-clock architecture
- 4K cache tags, physically tagged, virtually indexed
- Full MP support (Level 2 MBus)
- Block Copy/Fill support
- 800K transistors


**CY7C625 Block Diagram**

- IMB Control
- Address Translation Cache (64 Entry CAM)
- PTPC
- CMTU Registers
- Read Buffer
- MBus Control
- CMP
- CTAG (4K Entry)
- Asynchronous Bus Control
- MMU and Cache Control
- Write Buffer

**CY7C625 Clocking Schemes**

- **Synchronous**
  - IMCLK inverted MCLK

- **Asynchronous**
  - 2 IMCLK + 2 MCLK penalty
**CY7C625 Block Copy/Fill**

- Fully utilizes Read/Write buffers
- Block Copy copies 32-byte block from cache or main memory to another location in main memory
- Double word pattern written to 32-byte block in main memory
- Prevents these non-CPU intensive tasks from having to be brought into the cache

**CY7C627 Cache Data Unit**

- 16K X 32 synchronous SRAM
- On-chip address and data latches
- 1-stage write pipeline
**CY7C627 Block Diagram**

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**hyperSPARC Manufacturability**

- **Conservative Design**
  - 6T memory cells
  - Manageable die sizes
  - Fully static design
  - High yields
  - Fast clock frequencies
    - $66.7$ MHz

- **0.65μ CMOS**
  - Double layer metal
  - Designed to shrink to 0.5μ
hyperSPARC TAB Modules

AVAILABLE WITH ONLY
IN THIS FORM FACTOR