R4200 (Codename ICE)

A high-performance MIPS microprocessor for portables

Barb Zivkov,
MIPS Technologies Inc.

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Introduction and agenda

1/ R4200 Program objectives

2/ Key features

3/ Feature comparison
1. **R4200 Program Objectives**

*Design for portables*

- Low power
  
  \( \leq 2 \text{ watts} \)

- Low cost
  
  \( \leq $100 \)

- Small die size
  
  \( \leq 100 \text{ sq. mm} \)

- High performance
  
  \( \geq 50 \text{ SPECint92} \)

- Modular design
  
  (Megacell capable)

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**R4200 Floorplan**

![R4200 Floorplan Diagram](image-url)
Low Power:

- Designed for 3.3 volts
- Caches organized in banks
- Writeback cache
- Instruction cache Prefetch buffer
- Instruction micro-TLB
- Unified datapath
- Power management capability

Low Power (continued):

How does power management work?

- For reduced system activity, switch to RP mode
  - RP "reduced power" mode dissipates 0.4W
  - processor slows to 1/4 of normal frequency
  - no sacrifice in functionality
  - dynamically initiated by external agent / software

- For low system activity, switch to instant-off mode
  - instant-off mode dissipates 0 power
  - save processor state, flush cache
  - save/restore completed in milliseconds
Low Cost:

- Volume price near $70
- Small die-size (76 sq. mm)
- Plastic 208-pin QFP packaging
- High yields (column redundancy in caches, conservative design methodology)
- High-volume mass production

High Performance:

- 55 SPECint92 & 30 SPECfp92 (simulated with 256 KB write-through L2 cache)
- 50 SPECint92 & 28 SPECfp92 (simulated with no L2-cache)
- 160 MB/sec (sustained) System Interface
- Low latency for primary cache miss
R4200 - Modular design

Easy to...

- Increase/decrease caches
- Increase/decrease TLB
- Change system interface
- Offer core as megacell
- Generate derivative designs

R4000 / R4400 Compatibility:

- Full MIPS-III instruction set
- Full User-/Supervisor-/Kernel-level compatibility
- R4000 / R4400 compatible system interface
- R4000PC / R4400PC compatible packaging option, 179-pin GPGA (R4200PC)
2/ R4200 key features:

Wise allocation of resources:

- Traditional RISC pipeline
- Large on-chip caches
- Unified datapath
- Focused subset of R4000/R4400
- Detailed facts and figures

Traditional RISC pipeline

- 5 stages (IC->RF->EX->DC->WB)
- Shorter stalls
- Simpler control
- No branch interlock/penalty (one architecturally defined delay slot)
- More efficient at low clock frequencies (less power)
Large on-chip caches

- Instruction cache design
  - 14-bit index (16Kbyte cache)
  - 8-word line size, 4T RAM cells
- Writeback reduces system activity (low power)
- Organized in banks; only 1 bank powered on in any 1 access for power reduction (2 MSB's select bank)
- 1 cache access, 2 sequential instructions fetched (further reduces power)
- High hit rate (96.4% hit rate)
- 1 cache on SPECint92
- Column redundancy for improved yields

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R4200 - Unified Datapath

- Separate registers, shared datapath
- Less die area, lower cost
- Less capacitance, lower power
- Multicycle execution for Multiply, Divide, FP instructions with variable latencies

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**R4200 Unified datapath (contd.):**

**What are these variable latencies?**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Int(32)</th>
<th>Int(64)</th>
<th>FP(SP)</th>
<th>FP(DP)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add/sub</td>
<td>1</td>
<td>1</td>
<td>2.3</td>
<td>2.3</td>
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<tr>
<td>Multiply</td>
<td>13</td>
<td>24</td>
<td>2.11</td>
<td>2.20</td>
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<tr>
<td>Divide</td>
<td>37</td>
<td>69</td>
<td>2.29</td>
<td>2.58</td>
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<tr>
<td>Sqrt</td>
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<td>2.30</td>
<td>2.59</td>
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<tr>
<td>Abs/neg</td>
<td>-</td>
<td>-</td>
<td>1.1</td>
<td>1.1</td>
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<tr>
<td>Compare</td>
<td>-</td>
<td>-</td>
<td>1.1</td>
<td>1.1</td>
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<tr>
<td>DP→SP</td>
<td>-</td>
<td>-</td>
<td>2.2</td>
<td>2.2</td>
</tr>
<tr>
<td>SP→DP</td>
<td>-</td>
<td>-</td>
<td>1.1</td>
<td>1.1</td>
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<tr>
<td>FP→Int</td>
<td>-</td>
<td>-</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td>Int→FP</td>
<td>-</td>
<td>-</td>
<td>2.5</td>
<td>2.5</td>
</tr>
</tbody>
</table>

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**R4200 Focused configuration**

- Primary cache support only
- No MP support
- 2 page sizes supported (4KB & 16MB)
- Fixed cache line sizes (Inst. – 8 words; Data – 4 words)
R4200 Detailed facts & figures

Product configurations:  R4200LP, R4200PC
Die size:  8.8mm x 8.6mm
Process technology:  0.6 micron, 3 layer metal, 2 poly
Clock rates: (external/internal) 40/80 MHz (normal), 10/20 MHz (reduced power)
Transistor count:  1.3 million
Packages:  208-pin PQFP, 179-pin C-PGA
On-chip I-cache:  16 kilobytes w/ 8-word line
On-chip D-cache:  8 kilobytes w/ 4-word line
Supply voltage:  3.3 volts +/- 10%
Power consumption:  1.5W (normal); 0.4W (reduced)
On-chip integration:  Combined CPU/FPU, I-cache, D-cache, MMU w/ 32 double-entry TLB, 64-bit interface bus, Power management features, Graphics must suite

3/ Feature comparison:
How does R4200 compare to other processors?

- Implementation data

- Performance data
## R4200 Implementation data

<table>
<thead>
<tr>
<th>Processor</th>
<th>Size (sq. mm)</th>
<th>Micron/metal</th>
<th>Primary cache</th>
<th>Approx. cost</th>
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</thead>
<tbody>
<tr>
<td>R4000SC</td>
<td>184</td>
<td>0.8 / 2</td>
<td>8K Inst.</td>
<td>$600</td>
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<tr>
<td>R4400SC</td>
<td>184</td>
<td>0.6 / 2</td>
<td>16K Data</td>
<td>$1100</td>
</tr>
<tr>
<td>i486 DX/2 66</td>
<td>82</td>
<td>0.8 / 3</td>
<td>8K (Unified)</td>
<td>$500</td>
</tr>
<tr>
<td>Pentium</td>
<td>294</td>
<td>0.8 / 3</td>
<td>8K Data</td>
<td>$1000</td>
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<tr>
<td>PowerPC</td>
<td>121</td>
<td>0.6 / 4</td>
<td>16K Data</td>
<td>$400</td>
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<td>MicroSPARC</td>
<td>225</td>
<td>0.8 / 3</td>
<td>4K Data</td>
<td>$200</td>
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<tr>
<td>Hobbit</td>
<td>73</td>
<td>0.6 / 2</td>
<td>3K Data</td>
<td>$35</td>
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<tr>
<td>R4200</td>
<td>76</td>
<td>0.6 / 3</td>
<td>16K Data</td>
<td>$70</td>
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## R4200 Performance data

<table>
<thead>
<tr>
<th>Processor</th>
<th>MHz</th>
<th>SPEC92</th>
<th>Power</th>
<th>SPECint92/watt</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Ext/Int</td>
<td>Int</td>
<td>FP</td>
<td>Watts</td>
</tr>
<tr>
<td>R4000SC</td>
<td>50/100</td>
<td>62</td>
<td>63</td>
<td>12</td>
</tr>
<tr>
<td>R4400SC</td>
<td>75/150</td>
<td>94</td>
<td>105</td>
<td>15</td>
</tr>
<tr>
<td>i486 DX/2 66</td>
<td>33/66</td>
<td>32</td>
<td>16</td>
<td>7</td>
</tr>
<tr>
<td>Pentium</td>
<td>66</td>
<td>64</td>
<td>57</td>
<td>20</td>
</tr>
<tr>
<td>PowerPC</td>
<td>66</td>
<td>45</td>
<td>70</td>
<td>9</td>
</tr>
<tr>
<td>MicroSPARC</td>
<td>25/50</td>
<td>23</td>
<td>18</td>
<td>4</td>
</tr>
<tr>
<td>Hobbit</td>
<td>25</td>
<td>82</td>
<td>8?</td>
<td>0.4</td>
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<tr>
<td>R4200</td>
<td>40/80</td>
<td>55</td>
<td>30</td>
<td>1.5</td>
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</tbody>
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