AN INTEGRATED SOLUTION FOR
CT2 DIGITAL CORDLESS TELEPHONES

The Am79C410 PhoX™ Chip

PROGRESSION of CORDLESS TELEPHONY
(European Model)

DECT
HIGH PERFORMANCE
DIGITAL
BUSINESS
PBX, TELEPOINT

CT2
LOW COST DIGITAL
RESIDENTIAL,
TELEPOINT, PBX

CT1
ANALOG
RESIDENTIAL

CT0
ANALOG
RESIDENTIAL

Digital Variants:
CT2Plus
Simple DECT
CT2 APPLICATIONS

RESIDENTIAL TELEPHONES

OFFICE PBX SYSTEMS

PUBLIC TELEPOINT NETWORKS

BASIC CT2 HANDSET FUNCTIONS

Mic

Analog Front End

ADPCM Codec

Rate Conversion

Baseband Transceiver

RF Front End

Man-Machine Interface

(Keys, LED's, LCD, etc).

8-bit Microcontroller

Data Memory (RAM)

Program Memory (ROM)

Antenna

Battery

Data Memory (RAM)

Battery Power Management
INTEGRATED TECHNOLOGIES

- Analog (audio) Signal Processing
- Analog <-> Digital Conversion
- Digital Signal Processing (DSP)
- Voice Data Compression (ADPCM)
- Direct Digital Waveform Synthesis
INTEGRATED TECHNOLOGIES

- Digital CMOS "ASIC" Design
- 8-bit CMOS Microcontroller
- Memories: Static RAM and FIFO
- 3-5 V Power Supply
- Battery Back-up
- Integrated Power Management

THE PhoX CHIP DIE

Vital Statistics:
- Process: 0.8 um CMOS
- Die Area: 80k sq mils
- #Transistors: 200k
- Power Supply: 2.7 - 5.5 V
- Active Power @3V: 38 mW
- Standby @3V: 100 uW
ANALOG FRONT END

IN1
NETWORK

SQUARE WAVE GEN

15 dB

DSP 7-bit DAC

IN2
MICROPHONE

42 dB

OUT1
NETWORK

A/D DSP

OUT2
EAR

42 dB

SIDETONE

OUT3
LOUD SPEAKER

42 dB

DATA CONVERSION

A-D Converter:
Delta-Sigma Modulator Architecture
2 MHz Sampling Rate
1-bit Output
* High sampling rate makes anti-aliasing filters easy.

D-A Converter:
8-bit Resolution
128 kHz Sampling Rate
* High sampling rate makes output images easy to filter.
DSP and VOICE COMPRESSION

Transmit Analog (microphone) → A/D → Decimator (reduces sampling rate) → Bandpass Filter → Variable Gain → ADPCM Encoder → 32 kbps ADPCM

Receive (ear) Analog → D/A → Interpolator (increases sampling rate) → Lowpass Filter → Gain Variable → ADPCM Decoder → 32 kbps ADPCM

Tone Generation

Noise Detection/Suppression

DATA RATE CONVERSION

Aux. ports

Codec ADPCM Data 32 kbps

MUX → 32 kHz/32 kbps ADPCM Data

FIFO

32 kHz/32 kbps Burst Mode Data

FIFO

DSP Frame Timing

Clock Recovery and Digital Phase Locked Loop

Receive Data from Radio Link → Clock Recovery and Digital Phase Locked Loop → CT2 Frame Timing → CT2 Bit Timing
CT2 BASEBAND TRANSCEIVER

GMSK MODULATOR

GMSK - Gaussian-filtered Minimum Shift Key, a Frequency Shift Keying Technique for minimum spectral spread.

DDS - Direct Digital Synthesis:
Reduces part-to-part variation
Mask-programmed frequency response,
in this case a 6th-order Bessel filter
LOW POWER DESIGN

Low power is IMPERATIVE in a hand-held design

- 3 V Capability
- Full CMOS Design
- Special Low Power and "Zero Power" Modes
- Optimized DSP Engine
- Variable Processor Clock Rates
- Battery back-up input for static RAM
- Separate Enable Controls for Various Internal Peripheral Blocks

RAPID TIME TO MARKET

Rapid time to market is KEY to customer success in consumer industries.

- Parallel Development Paths
  - Software
  - Baseband Hardware
  - RF Hardware
- In-Circuit Emulation Capability for Software Design
- Test Injection/Detection Ports for Software Error Testing
- Audio Test Loopback Paths for Analog and Bit Error Rate Testing
- Direct Transmit Modulator Drive for RF Transmission Testing
PhoX CHIP CHALLENGES

- High Integration
- Diverse Silicon Requirements
- Low Power
- Variable Supply Voltage
- Built-in Development Support
- LOW COST