Research Project Goals

This chip is the result of a project with three interrelated goals:

- Develop expertise in custom ECL microprocessor design
- Develop high-performance microprocessor packaging
- Develop CAD tools for synthesis and analysis of VLSI ECL

Some non-goals included:

- Implementation of floating-point or virtual memory
- Multiprocessor support
- Highest SPECmark
Research Prototype Overview

Process 1μm single-poly
Devices 486K BJTs, 206K resistors
Internal power supply -5.2V, 21.2A
Input termination supply -2V, 4.8A
Data cache 2KB
Instruction cache 2KB
Package 504 pin, 366 signal
On-chip Clock 300Mhz
Power 115W

One Perspective on 115W

Sum of all chip powers disclosed at Hot Chips '92:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Alpha</td>
<td>30W</td>
</tr>
<tr>
<td>HP</td>
<td>20W</td>
</tr>
<tr>
<td>Spacle</td>
<td>2W</td>
</tr>
<tr>
<td>LSI graphics</td>
<td>4W</td>
</tr>
<tr>
<td>ARM</td>
<td>1W</td>
</tr>
<tr>
<td>SPARC90</td>
<td>1W</td>
</tr>
<tr>
<td>CM5 vector</td>
<td>5W</td>
</tr>
<tr>
<td>Fujitsu uVP</td>
<td>5W</td>
</tr>
<tr>
<td>Intel NIC</td>
<td>3W</td>
</tr>
<tr>
<td>Intel MRC</td>
<td>2W</td>
</tr>
<tr>
<td>Total given</td>
<td>73W</td>
</tr>
</tbody>
</table>

Note: 9 chips did not list their power dissipation!
**High Power <> High Temperature**

Numerical model of die temperature:

How is the chip cooled?

- safety cap
- seal ring
- condenser
- seal ring
- thermosiphon
- electrically testable assembly
- boiler
- film adhesive
- die
- PPGA
- bondwires
- lid
Package Electrical Issues

Plastic pin grid array.
50 ohm traces.
Termination resistors for all inputs are on-chip:

\[
\text{Power\_per\_input} = \frac{V^2}{R} = \frac{1.2^2}{50} = 28.8\text{mW}
\]

With 202 inputs, this accounts for 5.82W.
Processor Organization

Die Photo Before TAB Gold
**On-chip Cache Organization**

Both 2KB instruction and data caches:
- Have 16B lines.
- Have byte parity.
- Are direct-mapped.

The data cache is write-through.

In both caches, parity errors are converted to cache misses.

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**300Mhz!**

**Custom ECL vs. CMOS:**

\[ time_{wire} \propto \frac{V_{swing} \times C}{I_{drive}} \]

Custom ECL:
- Minimizes both \( V_{swing} \) and \( C \)
- Maximizes \( I_{drive} \)

Voltage swings on-chip:
- Single-ended: 575mV
- Differential: 230mV
- Cascode: 70mV
"Squeaky Clean" ECL

Every millivolt counts!

Each term in the noise budget is verified before tapeout.

21A Internal Supply Current

Gold bus bars supply large currents with low IR drops.

Entire die is covered with gold bus bars.

Inner row of pads on long sides are all Vcc and Vee1.

Power pads are bonded with 1.8mil gold bond wires.
Die with TAB Gold

IR Drops on Vee1

Power supply network extracted from layout and modeled:

Maximum drop is 14.5mV.
Clocking

On-chip phase-locked loop generates a high frequency chip clock from a low frequency board clock.

Any multiple of 1X to 8X the board clock can be generated.

A typical board clock is 75Mhz (4X).

All I/O pads have flip-flops clocked with the board clock.

No signals running at the chip clock frequency cross the package.

Testing

All on-chip flip flops and pad ring flip-flops have scan.

Scan is a small overhead in ECL.

Since the entire die is covered with 1 mil thick gold bus bars, scan is very important for debugging of the design.
**External Interface Overview**

The external interface is dominated by large unidirectional busses. These work in conjunction with a pipelined board cache. Each bus transitions every board clock. Tags and data are independently accessed during writes. Read bandwidths up to 4.8GB/sec, 1.2GB/sec typical. Write bandwidths up to 2.4GB/sec, 0.6GB/sec typical.

**Diagram:**

- **CPU chip**
- **Board cache tags**
- **Board cache data**
- **Refill data from main memory**
- **Clock signals (clk)**
**External Interface Timing**

Example: 3 writes to different 8B addresses followed by an instruction cache miss:

<table>
<thead>
<tr>
<th>Time</th>
<th>Cycle</th>
<th>To tags</th>
<th>Cache tags</th>
<th>From tags</th>
<th>On-chip control</th>
<th>To data</th>
<th>Cache data</th>
<th>From data</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>Probe #1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Probe #2</td>
<td>Probe #1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>Probe #3</td>
<td>Probe #2</td>
<td>Probe #1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>Probe #3</td>
<td>Probe #2</td>
<td>Probe #1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>I miss</td>
<td>Probe #3</td>
<td>Probe #2</td>
<td>I miss</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>I miss</td>
<td>Probe #3</td>
<td>Write #1</td>
<td>I miss</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>I miss</td>
<td></td>
<td>Write #2</td>
<td>Write #1</td>
<td>I miss</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
<td></td>
<td>Write #3</td>
<td>Write #2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Write #3</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CAD - Synthesis**

The chip was designed largely with CAD tools developed by the design team.

The schematics are graphical representations of C++ programs.

The design consists of 554 different cells:

- 93 are hand-drawn.
- 461 are automatically generated.
**CAD - Analysis**

Switch-level simulation of entire extracted layout, including the caches.
Performance tuning with a bipolar transistor-level timing analyzer.
Voltage drops on power supply and reference networks were calculated.
Noise margins and saturation margins on all circuits were verified.

**Conclusions**

Custom ECL enables:
- 300Mhz operation with 1μm feature sizes (circa 1990)
- Logic density comparable to custom CMOS
- Processor cost similar to CMOS microprocessor cost; not mainframe CPU cost