A Compact 3D Graphics Chip Set

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Outline

Design goals, objects, target markets/applications
3D graphics architectural approaches
Leo (ZX) system overview
The individual Leo chips: LC, LF, LD, LX
Design environment
Performance
Leo Deign Goals

- Complete single board subsystem solution for complex 3D graphics applications: mechanical CAD, bioCAD, scientific visualization, animation, entertainment, and virtual reality
- Acceleration of 3D Z-buffered rendering primitives: shaded triangles, antialiased vectors and dots, depth cueing
- Acceleration for X11 Windowing operations
- 1280×1024 76Hz display, double buffered 24-bit color with 24-bit Z-buffer, 8-bit overlay
- Full stereo video support

Example rendering: “Traffic Jam to Point Reyes”

Objects courtesy of Viewpoint Animation Engineering
Generic graphics pipeline

- Data Input
- Transformation
- Clip Test
- Face Determination
- Lighting
- Clip (if needed)
- Perspective Divide
- Screen Space Conversion
- Set Up for Incremental Render
- Edge-Walk
- Span-Interpolate
- Z-Buffered Blend
- VRAM Frame Buffer
- Double Buffered MUX
- Output Lookup Table
- Digital to Analog Conversion

Floating-point Intensive Functions

Drawing Intensive Functions

Generic parallel graphics pipeline implementation

1. Data Input
2. FIFO
   - Transform etc. Unit
3. FIFO
   - Transform etc. Unit
4. FIFO
   - Transform etc. Unit
5. FIFO
6. FIFO
7. FIFO
8. 2D Rendering
9. Frame Buffer Memory
10. Video Output

Note: The diagram illustrates the flow of data and processing stages in a generic graphics pipeline and a generic parallel graphics pipeline implementation.

Additional information: The diagram includes references to specific components and stages such as convolution and rendering, which are part of the graphics pipeline process.
Leo Block/Chip Diagram

LeoCmd Block Diagram

DMA
SPARC Reference MMU
LeoFloat Scoreboard

Bus Interface
Bucket Buffer
Format Conversion
Vertex Buffer
Output Formatter

BLIT ROP FONT
LeoCmd Feature List

- SBus DMA master
- SBus memory device
- Numerical format conversion of input data
- Converts chained graphics primitives to isolated graphics primitives
- Parallel X11 2D graphics port: BLIT, ROP, FONT
- Subsystem controller, scoreboards LeoFloat Array

LeoFloat

[Diagram showing the connection between input and output buses, control signals, and the microcoded floating point core.]
**LeoFloat Function Units, Register Files, and Data Paths**

Input from off-chip

\[ \text{IO} \rightarrow \text{P0} \rightarrow \text{R0} \rightarrow \text{CO} \]

\[ \text{IO}' \rightarrow \text{P31} \rightarrow \text{P63} \rightarrow \text{P64} \rightarrow \text{P91} \]

\[ \text{P64} \rightarrow \text{FMUL} \rightarrow \text{IALU} \rightarrow 1/X \]

**LeoFloat Execution**

<table>
<thead>
<tr>
<th>Inst Fetch</th>
<th>Inst Decode /branch</th>
<th>Register Fetch</th>
<th>ALU Functions (1-11 clks)</th>
<th>Register Store</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

Execute Pipeline

\[ d = a \times b + c; \]

Micro assembler syntax
LeoFloat Features

- Double Buffered I/O register files
- 288 Internal Registers
- Parallel IEEE FMul, FALU, 1/X, IALU
- Special 3D clip test instructions
- Dozens of specialized Condition code bits
- Dozens of specialized branch instructions
- Y-sort register instructions re-orders R registers
- Software pipeline scheduling
- 128K 32-bit word external microcode SRAM

The VRAM Bottleneck

- VRAM minimum
- Z-buffer RGB
- read/modify/write
- cycle time (on page)

- 100 pixel triangle
- theoretical
- maximum
- render rate per second

- 1 Meg VRAM
- 2 Meg VRAM
- 4 Meg
LeoDraw Features

- Renders Triangles
- Renders aliased and anti-aliased lines
- Renders aliased and anti-aliased dots
- Variable alpha blend & screen door transparency
- Per-pixel depth-cueing of all 3D primitives
- 3D pick box, DMA pick support
- 2D BLIT, ROP, FONT, pixel support
- Very fast screen clear, optimized vertical scroll
- Controls VRAM and DRAM

LeoCross Features

- Multiple color look-up tables
- “Cross bar” channel switching
- 32×32 cursor
- Video Timing, VRAM shift control
- Stereo and Virtual Reality device support
Design Environment

Genisil 8.1 for LeoCommand, LeoFloat, LeoDraw
.8μ double metal one poly CMOS
LSI 100K master slice for LeoCross
25 MHz target for Genisil chips, 67 MHz for LeoCross
Complete high level simulator written in C
Zycad gate level simulation for individual chips & whole system
3 of 4 chips completely functional first pass
Board up and rendering 3D images within days of receipt of chips

IC Details

<table>
<thead>
<tr>
<th>Chip</th>
<th>#gates</th>
<th>#transistors</th>
<th>die size</th>
<th>#pins</th>
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<tbody>
<tr>
<td>LeoCmd</td>
<td>83K</td>
<td>294K</td>
<td>580</td>
<td>240</td>
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<tr>
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<td>80K</td>
<td>280K</td>
<td>575</td>
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<td>LeoDraw</td>
<td>77K</td>
<td>270K</td>
<td>520</td>
<td>208</td>
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<tr>
<td>LeoCross</td>
<td>35K</td>
<td>-</td>
<td>460</td>
<td>416</td>
</tr>
</tbody>
</table>
The Leo board set: 5.7" × 6.7" × 0.6"

Performance

The Leo system achieves:

- 310K chained, un-lit, Gouraud shaded, Z-buffered 50 pixel depth-cued 3D triangles per second
- 250K isolated, lighted, Gouraud shaded, Z-buffered, 50 pixel depth-cued 3D triangles per second
- 750K chained, Z-buffer 10 pixel depth-cued 3D vectors per second
- 450K antialiased, isolated, Z-buffered, 10 pixel depth-cued 3D vectors per second
- 1.1M antialiased depth-cued 3D dots per second
- 143K 8×10 raster characters per second
- under 200ns window clear time

Note: all 3D performance benchmarks are averaged over many different orientations of the primitive.