A 500-MHz, 32-b, 0.4-μm CMOS RISC Processor (GALLOP)


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OUTLINE

1. Challenge
2. Chip photo and main features
3. Architecture for high speed processor
4. Key circuit techniques and experimental results
5. Summary
CHALLENGE

Making a high speed processor

- Fabrication technology  0.4 μm CMOS
- Design of high speed function blocks
- High speed oriented architecture
- Integration techniques for high speed function blocks

MAIN FEATURES & CHIP MICROPHOTOGRAPH

Fabrication technology
0.4- μm CMOS 3-level Al

Chip size
7.90 mm × 8.84 mm

Number of transistors
201,478

Power supply
3.3 V

Power dissipation
6 W at 500 MHz
ARCHITECTURE FOR HIGH SPEED PROCESSOR

- 8-stage pipelined datapath
- Simple datapath control
  - No pipeline hold
  - No register forwarding
- Testing

ARCHITECTURE

Clock → PLL 500 MHz

I-cache

DEC & CNT

ADD

CMP

BSFT

ADD

LU

RF

DREG

D-cache

Address bus

30

Data bus

32

Pipelining
SIMPLE CONTROL - NO PIPELINE HOLD

★ Instruction cache misses on operation "B"

I1

A B C D ⨿ .... X B C

I2

A B C ⨿ .... X X B C

RF

A B X[B] ⨿ .... X[B] X X B C

E1

A X X ⨿ .... X X X B C

E2

A X X ⨿ .... X X X B C

D1

A X ⨿ .... X X X X B C

D2

A X ⨿ .... X X X X B C

WB

× kill

SIMPLE CONTROL - SEQUENCER

Only cancellation of writing RF & D-cache is essential to killing instruction.
NO REGISTER FORWARDING

DATA HAZARD

Id $2, 0[$3]
addi $2, $2, 1

Instruction comparison

Register address comparison

FORWARDING

PENALTY FOR HIGH SPEED

<table>
<thead>
<tr>
<th>5-stage datapath</th>
<th>0.97 (CPI = 1.03)</th>
<th>280 MHz</th>
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<tbody>
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<td></td>
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<td>270 MIPS</td>
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<table>
<thead>
<tr>
<th>8-stage datapath</th>
<th>0.65 (CPI = 1.53)</th>
<th>300 MHz</th>
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<tr>
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<td>196 MIPS</td>
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Delete register forwarding | 0.57 (CPI = 1.75) | 285 MIPS |
|                           |                   | 500 MHz  |

* CPI data is estimated from J.L. Hennessy & D.A. Patterson
  "Computer Architecture: A Quantitative Approach", Appendix C
Simpler datapath control

Easily decoding instruction
ex. VLIW

Encoding register forwarding operation in instruction
for implementing register forwarding handling

Minimize the number of hold-stages

Using pipeline sequencer

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<th>B</th>
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<th>D</th>
<th>E</th>
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<td>I1</td>
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<tr>
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Hold 3 stages

Data hazard occurs in "A" and "B". Minimizing the number of hold-stages reduces the loads of the control circuits.

× kill
**KEY CIRCUIT TECHNIQUES**

- Stable power and ground lines
- High-frequency PLL clock generator
- Small-skew clock distribution strategy
- High-speed input and output buffer circuit
POWER & GROUND LINES

Power supply voltage bounce

Total decoupling capacitance on chip 0.027 μF

PLL CLOCK GENERATOR

Requirements for PLL
500-MHz output
Small output jitter

External clock → Phase Detector → Loop filter [Small jitter] → Voltage-controlled oscillator [500-MHz oscillation] → Frequency divider [500-MHz operation] → Internal clock
EXPERIMENTAL RESULTS OF PLL

PLL output waveform

Input 62.5 MHz
Output 500 MHz
1 V/div.
5 ns/div.

Output Jitter
Output jitter 58 ps (3%)
(This signal is 1/16 pre-scaled.)

CLOCK DISTRIBUTION STRATEGY

Data path
Cache
Phase-adjusting capacitors
Clock driver
Stage-connecting wire
PLL
Cache
CLOCK SKEW ON CHIP

Clock distribution tree on chip

PLL

Datapath block

skew 170 ps
4 V
0.5 ns

skew 100 ps
4 V
0.5 ns

skew 110 ps
4 V
0.5 ns

I/O CIRCUITS

Output buffer

VDD
In
0.5 V
Out
GND

V_{OH} = 1 V
V_{OL} = 0 V

Input buffer

VDD
Ref
Out
50 Ω

GND

Control

Adjustable termination resistor

On chip

Outside package

0
1
0 4 8 12 16 [ns]

1.3.10
**SUMMARY**

- 500-MHz, 32-b, 0.4-μm CMOS RISC processor
- Architecture for high speed processor
  - 8-stage pipelined datapath
  - Simple datapath control using sequencer
  - No register forwarding in datapath
  - On chip test function
- High-speed circuit techniques
  - Power and ground line structures
  - PLL clock generator
  - Stage-connect clock distribution
  - High speed input and output buffer circuit