The new i960® Processor that offers More for Less, the i960® Jx Series

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80960 Architecture

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Introducing the i960® Jx CPU

- Feature Set
- Special Features
- Power Saving Features
- Performance Results
Feature Set: Summary

- Single cycle execution of RISC ops.
- 3-ported register file with bypass.
- Concurrent Multiply/Divide unit.
- Parallel Loads with integer and MDU pipelines.
- HW-supported complex addressing modes.
- 4-KB I-cache; 8-set Local Register Cache.
- 2-KB D-cache and 1-KB on-chip data RAM.

Feature Set: Summary (cont)

- 16 to 50+ MHz parts with Clock Doubler Mode.
- 28-41 VAX MIPS.
- 750K Transistors, 64mm² die size,
- 0.8-μm process 3-layer metal,
- 3.3V and 5V versions with 132-pin PGA/PQFP.
- Already Taped-Out; Availability in Late ‘94.
Feature Set: i960® JX CPU Diagram

Special Features: Addressing Modes

<table>
<thead>
<tr>
<th>Address Computed</th>
<th>Jx Support</th>
<th>HLL Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>off12</td>
<td>HW:1cyc</td>
<td>Gen 12-bit const</td>
</tr>
<tr>
<td>dsp32</td>
<td>HW:2cyc</td>
<td>x = global_addr</td>
</tr>
<tr>
<td>(ra)</td>
<td>HW:1cyc</td>
<td>x = *ptr</td>
</tr>
<tr>
<td>off12 + (ra)</td>
<td>HW:1cyc</td>
<td>x = local_addr</td>
</tr>
<tr>
<td>dsp32+(ra)</td>
<td>HW:2cyc</td>
<td>x = ptr-&gt;elt</td>
</tr>
<tr>
<td>(ra)+(rx)*sc2</td>
<td>μcode</td>
<td>x = p[i]</td>
</tr>
<tr>
<td>dsp32+(ra)+(rx)*sc2</td>
<td>μcode</td>
<td>x = as[i]-&gt;elt</td>
</tr>
<tr>
<td>dsp32 + (rx)*sc2</td>
<td>HW:1cyc</td>
<td>PIC code</td>
</tr>
<tr>
<td>dsp32 + (IP) + 8</td>
<td>μcode</td>
<td></td>
</tr>
</tbody>
</table>
Special Features: Fast Call / Return

- 16 Global Regs and "N" sets of 16 local Regs.

- Save & restore local Regs to Register cache.

- Wide paths to Register cache allows 6 cycle ops.

- When cache is full, Oldest sets "spilled" to memory.

- Sets reserved for high-priority interrupts to avoid spills.

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Special Features: New i960 Ops

- Conditional ops avoid branches for short flows:

```
c  fragment:  x = (a == b) ? y+y1 : z-z1;
ASM fragment:  cmpo  a,b
               addoe  y,y1,x
               subone  z1,z,x
```

- Subword compares avoid masking.
- Byte-Swap instruction.

Special Features: Memory Accesses

- 1-KB on-chip RAM for key data & interrupt vectors.
- Profiling compiler can move variables to this RAM.
- Built-in unaligned memory reference support.
- Supports Big & Little endian memory accesses.
- Multi-word LD/ST ops: bus bursting & code density.
**Power:** Fully static, low-power design

- Typical Power usage: 0.5 watt - 3.3v @ 33MHz.
- Enhanced-Scalar is less power than super-scalar.
- Predict memory ops, then power-up D-cache.
- Don't drive μROM when not executing μcode.
- Stop clocks of an idle unit instead of ignoring result.
- Multiplex Addr/Data bus: lower pin count & power.
- New HALT instruction can reduce power by 90%.
- Exit HALT by external interrupt or on-chip timers

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**VAX MIPS (Dhrystone 2.1)**

<table>
<thead>
<tr>
<th></th>
<th>JF 40Mhz</th>
<th>JF 33Mhz</th>
<th>JF 25Mhz</th>
<th>JA 33Mhz</th>
<th>JA 25Mhz</th>
<th>JD 50/25Mhz</th>
<th>JD 40/20</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIPS</td>
<td>33</td>
<td>28</td>
<td>21</td>
<td>26</td>
<td>20</td>
<td>41</td>
<td>33</td>
</tr>
</tbody>
</table>

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**IMAGING PERFORMANCE**

- KA-25: 1.4
- JF-25: 3.1
- JD-50/25: 4.4

Based on simulation of Postscript page "Golfer"
### Processor Summary

- **Low-Power**
  - 2K I-Cache
  - 1K D-Cache
  - 1x Core
  - 3.3 V Operation
  - 33 MHz Core/Bus
  - 80L960JA

- **2x Core**
  - to 40 Mhz
  - 4K I-Cache
  - 2K D-Cache
  - 1x Core
  - 3.3 V Operation
  - 40 MHz Core/Bus
  - 80L960JF

- **High-Performance**
  - 4K I-Cache
  - 2K D-Cache
  - 2x Core
  - 5.0 V Operation
  - 50 MHz Core
  - 25 MHz Bus
  - 80960JD

### Backup: Feature Table

<table>
<thead>
<tr>
<th></th>
<th>80L960JA</th>
<th>80960JF</th>
<th>80L960JF</th>
<th>80960JD</th>
</tr>
</thead>
<tbody>
<tr>
<td>I-Cache (2-way)</td>
<td>2K</td>
<td>4K</td>
<td>4K</td>
<td>4K</td>
</tr>
<tr>
<td>D-Cache/DataRam</td>
<td>1K / 1K</td>
<td>2K / 1K</td>
<td>2K / 1K</td>
<td>2K / 1K</td>
</tr>
<tr>
<td>Cached local reg sets</td>
<td>8 sets</td>
<td>8 sets</td>
<td>8 sets</td>
<td>8 sets</td>
</tr>
<tr>
<td>VAX MIPS</td>
<td>28 (33MHz)</td>
<td>33 (40MHz)</td>
<td>28 (33MHz)</td>
<td>41 (50MHz)</td>
</tr>
<tr>
<td>Clock (MHz)</td>
<td>16, 25, 33</td>
<td>16, 25, 33, 40</td>
<td>16, 25, 33</td>
<td>33, 40, 50</td>
</tr>
<tr>
<td>Clock Doubler mode</td>
<td>no</td>
<td>no</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>3.3v</td>
<td>5v</td>
<td>3.3v</td>
<td>5v</td>
</tr>
<tr>
<td>Typical Power</td>
<td>0.5W (33MHz)</td>
<td>1.2W (33MHz)</td>
<td>0.5W (33MHz)</td>
<td>1.9W (50MHz)</td>
</tr>
<tr>
<td>Availability</td>
<td>3/95</td>
<td>12/94</td>
<td>3/95</td>
<td>6/95</td>
</tr>
</tbody>
</table>

750K Transistors, 64mm² die size, 0.8-µm process
3-layer metal, 132-pin PGA/PQFP