SH2: A Low Power RISC Micro for Consumer Applications

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Why are RISCs in Consumer Market?

- The consumer market is huge
  - Children drive an $8,000,000,000 consumer electronics market
  - Video game revenue now exceeds movie revenue

- Compatibility is not an issue.
  - Currently no consumer electronics standard exists.

- Consumer products are becoming sophisticated.
  - Graphical user interfaces, 3D animation, imaging, complex communications protocols, object-oriented programming

- Price sensitivity is high
  - A $20 price reduction doubles video game sales
  - A $29 or lower price point is comensurate with children's spending capability
SH Family History

Introduced in 1992

Two versions available now
- SH1: embedded controller
- SH2: embedded processor with cache

Two versions under development
- SH3: embedded processor with cache and mmu
- SH4: embedded processor with cache, and multi-media extensions

Over 300 design wins to date
- Industry (41%), Consumer (25%), PC/Communications (20%), Automotive (14%).

Volume shipment started
- Consumer (60%), PC/Communications (15%), Automotive (14%), Industry (11%)
SH2 Architectural Features

- **16-bit Fixed-Length Instructions**
  - Unified data and instruction write through cache for performance with slow memories
  - Small object code footprint minimizes memory requirements and cache traffic
  - 32-bit instruction fetch allows data loads to be scheduled for non-conflicting access to the cache
  - Immediate data pooled in instruction stream

- **16 General Purpose Registers, 6 Special Purpose Registers**

- **DSP Capability (Multiply Accumulate)**
  - supports fixed-point $\sum a_i \cdot b_i$
  - 4 cycles for $32b \cdot 32b + 64b \rightarrow 64b$

SH2 On-chip Functions

- **Direct support for popular memory interfaces**
  - SDRAM, DRAM, PSRAM, Masked ROM, SRAM
  - 6 cycle cache fill (16-byte line) from SDRAM

- **32-bit Fixed-Point Multiplier for 3D coordinate transformations**

- **Free-running 64-bit/32-bit Division Unit for 3D perspective transformations**

- **DMAC, serial interface, timer, interrupt controller, and debugger interface**

- **Dual-Processor Configuration Support**

- **Software controlled phase-locked loop (PLL)**
SH1 / SH2 Features

Machine

*SH1*

- dhrystone 2.1: 16MIPS (28,112)
- Clock frequency: 20MHz @5V
- Operating voltage: 2.7V ~ 5.5V
- CPU core size: 5.90mm²
- Multiplier size: 1.40mm²
- On-Chip Memories: 64KB ROM, 4KB RAM
- On-Chip Peripherals: 4DMAC, 2serial, ITU, 8A/D
- DRAM controller
- Chip size: 8.67mm X8.67mm
- Power consumption: 500mW @5V
- Process technology: 2-metal 0.8 micron
- First silicon: September, 1992
- Package: 112 PQFP

*SH2*

- 25MIPS (45,477)
- 28.7MHz @5V
- 2.7V ~ 5.5V
- 5.45mm²
- 2.66mm²
- 4KB, 4-wayUnified$
- 2DMAC, Serial, DiV
- SDRAM/DRAM i/f, etc.
- 7.59mm X7.44mm
- 400mW @ 5V
- 2-metal 0.8 micron
- October, 1993
- 144 PQFP

HOT CHIPS VI

Smaller Object Size
(Further Improvement in Progress)

Data: courtesy of Cygnus Support.
All are measured with GNU CC

HOT CHIPS VI
**SPECint92 vs. Power**

![Graph showing SPECint92 vs. Power with various processors and their power dissipation.]

**SH2 Power Consumption Breakdown**

![Bar chart showing the power consumption breakdown for SH2 with specific components and their power usage.]

- **394mW**
  - External pins: 103mW
  - PLL+Clock: 21mW
  - Peripherals: 55mW
  - Memory Controller: 32mW
  - Cache: 54mW
  - Internal Buses: 35mW
  - CPU+Multiplier: 94mW
SH3 / SH4 Roadmap

<table>
<thead>
<tr>
<th>Machine</th>
<th>SH3</th>
<th>SH4</th>
</tr>
</thead>
<tbody>
<tr>
<td>dhrystone 2.1</td>
<td>60 / 100MIPS</td>
<td>300MIPS</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>60 / 100MHz @ 3.3V</td>
<td>200MHz @ 2.5V</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>2.2V ~ 3.6V</td>
<td>1.5V ~ 2.8V</td>
</tr>
<tr>
<td>Process technology</td>
<td>3-metal 0.5 micron</td>
<td>3-metal 0.35 micron</td>
</tr>
<tr>
<td>First silicon</td>
<td>1994</td>
<td>1995</td>
</tr>
</tbody>
</table>

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Conclusions

SH2 gives good performance with a small die size and vanilla process.
- 25MIPS processor and peripherals in 56 mm2 @ 0.8 micron
- First processor to include an SDRAM interface
- Example application: video game accelerator box.

SH2 was designed for consumer applications from the start.
- 16-bit instructions contribute to small object code size
- Unified cache and data path help to keep die small
- DSP capability improves voice, image and 3D processing performance
- Low power, Low EMI, and Low Cost Design
- Low power cache
- Small CPU core (5.42mm2 @ 0.8 micron)

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