82430NX PCISet: Companion to the Highest Performance Pentium™ Processor

Hot Chips VI Symposium

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Agenda

◆ Design Goals
◆ Architecture Overview
◆ Implementation Details
◆ Benchmark Results
◆ Summary
Design Goals

- Highest Performing Desktop System for the Pentium™ processor at iCOMP™ Index 815\100 MHz and Pentium processor - 735\90
- Uni- or Dual-Processor Designs with Maximum Performance and Minimum Complexity
- High Performance PCI Local Bus
- Enable Power Management on the Desktop
- Modular Architecture for EISA/ISA

82430NX Overview - Components

<table>
<thead>
<tr>
<th>Pentium™ processor - 815\100</th>
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</thead>
<tbody>
<tr>
<td>Host Bridge</td>
</tr>
<tr>
<td>PCMC - PCI/Cache /Memory Controller</td>
</tr>
<tr>
<td>LBX - Local Bus Accelerator (2 Devs)</td>
</tr>
<tr>
<td>EISA Bridge</td>
</tr>
<tr>
<td>PCEB - PCI-to-EISA Bridge</td>
</tr>
<tr>
<td>ESC - EISA System Controller</td>
</tr>
<tr>
<td>ISA Bridge</td>
</tr>
<tr>
<td>SIO - System I/O</td>
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PCI Bus

3.3 Volt Host Bus
82430NX System Diagram

◆ UP System with - ISA/EISA

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</tr>
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<td>DRAM</td>
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PCEB  ESC OR SIO
EISA/ISA BUS

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82430NX System Diagram

◆ DP System with - ISA/EISA

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PCEB  ESC OR SIO.A
EISA/ISA BUS

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82430NX Overview - Features

- Supports Pentium™ processor at iCOMP™ Index 815\100 MHz and Pentium processor - 735\90
- 256/512K WB Burst or ASync Second Level Cache
  - Option configurations for multiple price points
- Integrated Tag Ram
  - Board space and cost savings
- Dual Processing Support
- Power Management Support
- 133 MB/Sec PCI Bus Transfer Rate
  - Designed for highest performance PCI
- Optional ISA or EISA Standard Bus Interface

82430NX PCIset - Implementation Details

- PCIset Partitioning
- Optimized 3.3 Volt Host Bus Interface
- Dual Processing Capability
- Optimized L2 Cache/DRAM Controller
- High Performance PCI Local Bus Interface
- Power Management Support
- ISA/EISA Expansion Bus
82430NX PCIset - Partitioning

◆ Host Bus
  ■ PCI/Cache/Memory Controller (PCMC) - 208 pins, 2.0 W
  ■ Local Bus Accelerator (LBX) - Two 160 pins, 1.4 W
  ■ Both Components use 5 Volt core and 5V/3.3 V Buffers

◆ ISA Bridge
  ■ System I/O (SIO) - 208 Pins, 1.0 W

◆ EISA Bridge
  ■ PCI/EISA Bridge (PCEB) - 208 pins, 0.9 W
  ■ EISA System Controller (ESC) - 208 pins, 0.7 W

All Components are 0.8 micron in QFP Packages

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82430NX PCIset - 3.3V Host Bus

◆ Main Features
  ■ 64-Bit Data Path, 32 Bit Address w Pipelining
  ■ Synchronous Operation at 60/66 MHz
  ■ Burst Read/Write transfers to Cache/Memory

◆ Challenges
  ■ All Host Bus Clocks Routed With Sub 1ns Clock Skew
  ■ 66 MHz AC Analysis Provided Guidelines on Trace Lengths to meet Setup and Hold Requirements
  ■ 4-Corner Simulations Met with DP Reference Platform
82430NX PCIset: 3.3 Volt Power

- 3.3 Volt Power to PCIset and processors
  - Use separate 3.3V power plane or 3.3V island (below)
  - Power Supply: External or Voltage Regulated

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3.3 Volt Island

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5 Volt Power Plane

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82430NX System Board

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82430NX PCIset: 3.3 Volt Power

- PCMC/LBX have “Split Ring” Pinout
  - 5 Volts powers the Core, 3.3V powers the Host Bus I/F

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□ = 5V PIN
○ = 3.3V PIN

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3.3 Volt Plane

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82430NX PCIset: Dual Processing

- Signals Common on Host Bus
  - Address, Data, Control, and 66 MHz Host Clock
  - Added Signals are CPU Arb. Bus and APIC
- "0" Extra Pins required on PCMC for DP

```
+-----------------+    +-----------------+
| Pentium™ processor|-->| Pentium™ processor|
| - 815\100        |    | - 815\100       |
+-----------------+    +-----------------+
      |                          |
      v                          v
      Address, Data, Control     Address, Data, Control
                                       +-----------------+
                                       | PCMC             |
                                       +-----------------+
```

82430NX PCIset: Dual Processing

- I/O APIC Function is in the ESC or SIO.A
  - APIC Goal: Multiprocessor Interrupt Management
  - PCIset, BIOS, and O/S vendor follow MP Spec V1.1

```
+-----------------+    +-----------------+
| Pentium™ processor|    | Pentium™ processor|
| - 815\100        |    | - 815\100       |
| Local            |    | Local            |
| APIC             |    | APIC             |
+-----------------+    +-----------------+
      +-----------------+    +-----------------+
      | 3-wire bus       |    | 3-wire bus       |
      +-----------------+    +-----------------+
      | ESC or SIO.A     |    | I/O APIC         |
      +-----------------+    +-----------------+
      | 16 MHz Clock     |    | 2 Data Lines     |
      +-----------------+    +-----------------+
```

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82430NX PCIset - L2/DRAM I/F

◆ Second Level Cache
  ■ 256K or 512K Direct-Map Write Back Cache
  ■ Integrated Tag RAM for Board Space/Cost Reductions
  ■ Burst SRAM with 3-1-1-1 Read/Write Timing
  ■ Standard SRAM with 3/4-2-2-2 Read/Write Timing
  ■ Fully Concurrency with PCI and Main Memory
  ■ Byte Parity Optional

◆ DRAM Controller
  ■ Burst Line Fill
  ■ Cache Line Posting with 4-1-1-1 Timing
  ■ Up to 512 MB DRAM
  ■ Supports 5 Volt DRAM

82430NX PCIset - PCI Local Bus

◆ CPU-to-PCI Local Bus Interface
  ■ .133 MB/S PCI Local Bus Interface
  ■ CPU posts data to PCI in 3 clocks
  ■ "0-Wait State" 1 Clock Burst Writes on PCI

◆ PCI-to-Main Memory
  ■ PCI Masters Posts Data into Main Memory via Two 4 Dword Buffers
  ■ PCI Master Reads Data from Main Memory via 4 Quadword Buffer
82430NX Power Management

◆ Power Management Features

- **SMI# Interrupts**: take the hardware in/out of power managed state
- **SMM Space**: PCIset provides 64K byte of protected area for SMM Code
- **INTR Logic**: selectable by user to create power down/up events
- **STPCLK#**: toggles high/low to reduce power on the processor, but still “ON” enough to perform critical tasks

```
STPCLK#
```

```
time
```

82430NX Power Management

◆ Sources of System Management Intr. (SMI)

- **Sources to enter power-down mode**
  - FAST-Off Timer - driven by lack of interrupts
  - Software APM Interrupt
  - External “Power Management” Button

- **Sources to go to full power mode**
  - Interrupts, e.g. Keyboard or Mouse
  - Software APM Interrupt

```
Pentium™ processor - 815100
```

```
ISA or EISA BRIDGE
```

```
SMI#
```

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Results

This Foil Reserved for:

* Benchmark Results
* Power Management Measurements

Summary of Key Points

We Have:

* Highlighted 82430NX PCIset Features
* Reviewed 3.3 Volt Requirements
* Discussed Dual Processing
* Detailed 82430NX Power Management