A PCI Bridge Chip (MPC105) with a Cache and Memory Controller for PowerPC™ Microprocessor

Karl Wang, Chris Bryant, Mike Carlson, Tom Elmer, Adrian Harris, Mike Garcia, C. S. Hui, C. K. Leung, Brian Reynolds, P. O. Tang, Laura Weber, Jim Wenzel, Glen Wilson, Mike Becker

Somerset Design Center
Motorola Inc.

6501 William Cannon Drive West
Austin, Tx. 78735-8598

(512) 795-7136

Karlw@ibmoto.com@oakhill.sps.moto.com

PowerPC™ is a trademark of IBM Corporation

OUTLINE

• INTRODUCTION
• DESIGN FEATURES
• ARCHITECTURE
• PERFORMANCE
• PACKAGING
• SUMMARY
PC System Using MPC105 and PowerPC Processor

MPC105 Features

- Single chip.
- PowerPC Reference Platform (PReP) compliant.
- PowerPC 601, 603, 604 microprocessors.
- 32-bit address bus, 64 (or 32)-bit data bus.
- Direct mapped L2 cache (write-through, write-back).
- SMP upgrade.
- DRAM or SDRAM (1GByte).
- ROM (16MByte).
- Byte writes to flash EPROM (1MByte).
- Fully PCI compliant.
- Bi-endian support.
- Power management.
DRAM Memory Organization

8 Banks support memory with sizes up to 1 GByte

Secondary Cache System Block Diagram
Internal Buffering

Processor Interface Control Block

Memory Control Block

PCI Control Block

Copyback Buffer

Processor

Linefill

L2 Dirty Line

L2 Castout

MPC105

Copyback Buffer

Memory

32-Bytes

Copyback
PCI to Memory Read/Write Buffer

Memory

MPC105

32-Bytes  32-Bytes  32-Bytes

PCI

Processor to PCI Read/Write Buffer

Processor

MPC105

16-Bytes  16-Bytes  32-Bytes

PCI
Performance

<table>
<thead>
<tr>
<th>Transaction</th>
<th>Number of Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor-to-Memory</td>
<td></td>
</tr>
<tr>
<td>Burst read from L2</td>
<td>3-1-1-1</td>
</tr>
<tr>
<td>Pipelined burst read from L2</td>
<td>3-1-1-1/1-1-1-1-1</td>
</tr>
<tr>
<td>Burst write to L2</td>
<td>3-1-1-1</td>
</tr>
<tr>
<td>Burst read from DRAM</td>
<td>8-3-3-3</td>
</tr>
<tr>
<td>Burst write to DRAM</td>
<td>8-3-3-3</td>
</tr>
<tr>
<td>PCI-to-Memory</td>
<td></td>
</tr>
<tr>
<td>Pipelined Burst read</td>
<td>9-1-1-1-1-1-1-1-1/1-1-1-1-1-1</td>
</tr>
<tr>
<td>Pipelined Burst write</td>
<td>2-1-1-1-1-1-1-1-1/2-1-1-1-1-1-1-1</td>
</tr>
<tr>
<td>Processor-to-PCI</td>
<td></td>
</tr>
<tr>
<td>Single read</td>
<td>12</td>
</tr>
<tr>
<td>Single write</td>
<td>5</td>
</tr>
</tbody>
</table>

2 to 1 mode

Current VS Cycle Time

3.3V, 25 C
Motorola MPC105

PCI Bridge / Memory Controller for Power PC™

C4/CBGA Package Technology
SUMMARY

- PowerPC Reference Platform (PreP) compliant bridge between PowerPC microprocessor and PCI bus.
- PCI compliant.
- Integrated L2 cache and memory controller.
- Architecture optimized for performance.
- 0.5um, 4-level metal CMOS technology.
- Die size of 6.2mm x 5.7mm (39mm²).
- 247K devices.
- C4/304 pin Ball Grid Array.
- Worst case power dissipation of 2.6 W at 66 MHz.
- Power management.