PowerPC 604™ RISC Microprocessor

Marvin Denman
Somerset Design Center

Presentation Outline

- Overview
- Execution
- Branch Prediction
- Memory System
- Summary
Overview

- PowerPC™ 32-bit architecture
- Targeted for Next Generation Desktop
- Four-way superscalar
- Speculative execution
- Multiprocessor Support
- Projected performance @ 100 Mhz
  - 160 SPECint92™
  - 165 SPECfp92™
- 196 mm², 0.5 μm CMOS, 4 layer metal
- 3.6 Million transistors

Performance Strategy

- Dynamic branch prediction
- Speculative execution with rapid correction
- Register renaming to remove false dependencies
- Reservation stations for each execution unit
- Execution serialization for non-renamed resources
- Load and store queues
PowerPC 604 Microprocessor Block Diagram

Superscalar Speculative Execution Highlights

- 6 stage pipeline
  Fetch, decode, dispatch, execute, complete, writeback
- 8-entry instruction buffer (4 decode, 4 dispatch)
- Rename registers: 12 GPR, 8 FPR, 8 CR
- 16-entry reorder buffer
- 6 execution units
- 2-entry reservation stations on each execution unit
- Fast branch misprediction recovery
Branch Prediction Highlights

- 64-entry fully associative Branch Target Address Cache (BTAC)
- 512-entry 4-state Branch History Table (BHT)
- Prediction at fetch, decode, and dispatch stages
- Rapid misprediction correction
- Speculative execution past up to 2 branches
- Speculative fetching past up to 6 branches

Branch Prediction Organization

[Diagram showing the connection between BHT, BTAC, Decode Buffers, Decode Prediction, Dispatch Buffers, Dispatch Prediction, Reservation Stations, Execution Correction, Completion Correction, MUX, FAR, and To I-cache.]
**Memory Pipeline Highlights**

- 16 KB instruction and 16 KB data caches with parity
- Two 128-entry two-way set associative TLBs
- 6-entry store queue, 4-entry load queue
- 2-entry copyback queue with single cycle castout
- 2-entry data linefill buffer
- 1-entry instruction linefill buffer
- 2 cycle load on cache hits
- Loads can bypass stores
- Coherent data cache with dual ported tags for snoop
- Caches non-blocking on misses
Data Cache State Diagram
MESIA Protocol

Invalid I → Cache Miss → Allocate A
  Replace (copyback) → Replace → Share S
  Snoop-RWITM (copyback) → Reload-Share

Modified M → Snoop-Read
  Store-Hit → Replace
  Snoop-Read (copyback) → Reload-Exclusive
  Cache-Line Clean → Store-Hit

Exclusive E

Software / System Support

- Instruction and data address breakpoints
- Single step trace and branch trace
- Performance monitor
- IEEE 1149.1 JTAG
- Nap mode that continues to snoop
Summary

- High performance PowerPC Architecture™
- Highly advanced superscalar processor
- Can execute up to 4 instructions per cycle
- Highly speculative execution
- 6 execution units
- Non-blocking pipelines
- Efficient memory operations
- System support

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