The Thunder SPARC Processor

HOT Chips VI

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Metaflow Background

• Company founded in 1987
• Pioneers in out-of-order/speculative execution microprocessor design
• First major design contract was LSI Logic's "Lightning" SPARC chipset (completed 1991)
• "Thunder" SPARC 3-chip set is improved version of "Lightning" 4-chip set
• Project 100% funded by Hyundai Electronics
• Thunder chipset first silicon July 1993
• Patented out-of-order architecture
Thunder SPARC Mbus Module

Thunder SPARC Chipset

- Superscalar fetch, issue, and execution
- Dynamic scheduling (dataflow)
- Out-of-order execution
- Speculative execution
- Above “hidden” from the programmer
- Factor of 2-3 performance advantage from architecture
Microprocessor Hardware Trends

- Superscalar instruction issue
- Super-pipelined execution units
- Super-fast processor clocks (>100 MHz)
- Out-of-order execution
- Speculative execution

Out-of-Order Execution

<table>
<thead>
<tr>
<th>PROGRAM ORDER</th>
<th>COMPLETION ORDER</th>
</tr>
</thead>
<tbody>
<tr>
<td>float A, X, XX, X1</td>
<td>n = n + 1;</td>
</tr>
<tr>
<td>int n</td>
<td>X = X + A;</td>
</tr>
<tr>
<td>.</td>
<td>XX = A * A;</td>
</tr>
<tr>
<td>.</td>
<td>X1 = 1 / A;</td>
</tr>
<tr>
<td>X1 = 1 / A;</td>
<td>n = n + 1;</td>
</tr>
<tr>
<td>XX = A * A;</td>
<td>X = X + A;</td>
</tr>
<tr>
<td>n = n + 1;</td>
<td>XX = A * A;</td>
</tr>
<tr>
<td>X = X + A;</td>
<td>X1 = 1 / A;</td>
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<td>.</td>
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</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Operation</th>
<th>Clocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>FP divide</td>
<td>10</td>
</tr>
<tr>
<td>FP multiply</td>
<td>5</td>
</tr>
<tr>
<td>FP add</td>
<td>3</td>
</tr>
<tr>
<td>Integer add</td>
<td>1</td>
</tr>
</tbody>
</table>
Speculative Execution

\[ \sum_{i=0}^{n} \sqrt{X_i} \]

**C EXAMPLE**

```c
for ( i = 0; (i < MAX); ++i ) {
    if (X[i] < 0) error_exit();
    sum = sum + sqrt(X[i]);
}
```

Speculative execution opportunity

**FORTRAN EXAMPLE**

```fortran
DO 100 i = 1, max
    IF (X(i) .LT. 0) CALL error_exit
100 CONTINUE
```

Conventional Pipeline

![Conventional Pipeline Diagram]

FETCH

ISSUE

EXECUTE

RETIRE
Metaflow Pipeline (DRIS)

Metaflow DRIS Entry

Source Operand 1
Locked | RegNum | ID

Source Operand 2
Locked | RegNum | ID

Destination
Latest | RegNum | Instruction's Results

Dispatched  Functional Unit  Executed  Program Counter
Yes/No  Class Number  Yes/No  Content
Thunder Processor

Distinguishing Features

- 4 instructions issued per clock (3 integer, 2 floating point instructions and one branch)
- 8 parallel functional units (3 integer ALUs, 2 FP ALUs, 1 branch unit, 2 memory/bypass)
- Dataflow-based out-of-order instruction issue/execution (memory/ALU operations), in-order completion, precise traps and interrupts
- Speculative execution beyond unresolved conditional branches (multiple basic blocks with instant state repair on error)
- Above mechanisms transparent to executing program (strict SPARC V8 compatibility)
Thunder Unusual Features

• Eager evaluation ("folds" conditional branches)
• Multiple instances of memory locations ("memory renaming")
• Out-of-order memory references
  – Multiple simultaneous cache miss processing ("non-blocking cache")
  – Split address and data memory transactions (memory response re-ordering allowed)
• Speculative memory reads with respect to shared memory coherence restrictions (emulates "strong consistency" model)
• Uninterrupted transitions between user and supervisor modes (traps/interrupts)

Thunder Unusual Features
(continued)

Floating Point Unit (FPU)

• Variable latency FPU (early termination for divide/square root)
• Non-blocking divide and square root (concurrent add/multiply)

Branch Prediction

• Dynamic branch prediction
• Generalized loop count prediction
• Return-from-subroutine (RET) "folding"
• Jump-through-register prediction (JMPL cache)
Thunder Status

<table>
<thead>
<tr>
<th></th>
<th>Thunder 1.0</th>
<th>Thunder 1.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>First Silicon</td>
<td>July/Nov 1993</td>
<td>Q4 1994</td>
</tr>
<tr>
<td>Foundry</td>
<td>VLSI Technologies</td>
<td></td>
</tr>
<tr>
<td>CMOS technology</td>
<td>0.6/0.8 µm</td>
<td>0.5 µm</td>
</tr>
<tr>
<td>Metal layers</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>5V</td>
<td>3.6V</td>
</tr>
<tr>
<td>Clock rate (processor)</td>
<td>50 MHz</td>
<td>80 MHz</td>
</tr>
<tr>
<td>(Mbus)</td>
<td>40 MHz</td>
<td>≤60 MHz</td>
</tr>
<tr>
<td>Die Size (mm square)</td>
<td>14.5/16.5</td>
<td>9.1/11.8</td>
</tr>
<tr>
<td>Package</td>
<td>IPGA (391 pins)</td>
<td>TBGA (600+ pins)</td>
</tr>
<tr>
<td>Methodology (data path/RAM)</td>
<td>Full custom</td>
<td></td>
</tr>
<tr>
<td>(control logic)</td>
<td>Standard cell</td>
<td></td>
</tr>
<tr>
<td>(test)</td>
<td>JTAG/full scan</td>
<td></td>
</tr>
<tr>
<td>External cache RAM (type)</td>
<td>“Viking”</td>
<td></td>
</tr>
<tr>
<td>(size)</td>
<td>Eight 128K x 9</td>
<td>Eight 64K x 18</td>
</tr>
<tr>
<td>Total transistors (3 chips)</td>
<td>~6 million</td>
<td>~6 million</td>
</tr>
</tbody>
</table>

Thunder Performance Goals

![Graph showing SPECfp92 and SPECint92 performance over time]

- SPECfp92
- SPECint92

- 50 MHz 0.8/0.6 µm
- 80 MHz 0.5 µm
- 120 MHz 0.5 µm

Q1'94 Q4'94 Q2'95
Thunder 1.0 IU Floor Plan

Thunder 1.0 IU Die Photo
Thunder 1.0 CMB Die Photo