The MiniRISC™ CW4010:
A Superscalar MIPS Processor ASIC core

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MiniRISC CW4010 Agenda

- Design goals & initial decisions
- MiniRISC CW4010 overview
- Instruction set & internal organization
- Configuring for specific applications
- Software development support
- Evaluation device
- Performance
MiniRISC CW4010 Design Decisions (1)

- Target markets: high-performance embedded
  - Performance goal: at least 100 native MIPS
  - Combine CW4010 CPU core with building blocks and other logic to create single-chip systems.
  - Examples: games, set-top boxes, printers, routers.
  - Meet consumer product cost constraints.

- Minimize die area & power consumption
  - Combined die area of CPU and other logic must permit designs to meet cost constraints.
  - Total power budget must suit low-cost packaging, and portable battery-powered operation.

MiniRISC CW4010 Design Decisions (2)

- Modular design, easily customized
  - Building blocks included/excluded to suit application.
  - ASIC designer selects area vs. performance tradeoff.

- On-chip interfaces for easy extension
  - On-chip logic blocks can be defined for application-specific acceleration.
  - New blocks can connect to CW4010 as coprocessors.
  - New hardware can be supported by new user-defined instructions.

- Implemented in standard cell technology
  - Must be compatible with standard ASIC design flow.
  - Designs must suit LSI Logic's ASIC process flow.
MiniRISC CW4010 Design Decisions (3)

☐ ‘Conservative’ superscalar architecture.
  ✦ Multiple issue reduces reliance on high clock rate.
  ✦ Avoidance of aggressive architectural options allows more die area for user-defined logic.

☐ Moderate pipe depth (enhanced 5-stage).
  ✦ Avoids reliance on high-accuracy branch prediction.
  ✦ Enhancements reduce branch penalty below that of basic 5-stage pipe.
  ✦ Allows use of simple prediction scheme, saving area.

MiniRISC CW4010 Overview (1)

☐ 32bit Superscalar CPU
  ✦ 2 instructions per cycle (max)

☐ 110 native MIPS @ 80 MHz (160 MIPS peak)
  ✦ On a mix of small benchmarks - Dhrystone etc.

☐ Easily customized by ASIC designer
  ✦ Modular building blocks may be used selectively
  ✦ User-defined hardware attaches to onchip interfaces

☐ Compatible with R4000 32bit mode (MIPS-II)
  ✦ 32-bit addressing and integer instructions.
  ✦ CW4010-specific instruction set enhancements - improves performance in DSP applications.
MiniRISC CW4010 Overview (2)

- Dual internal 32-bit paths
  - 64-bit on-chip bus interface.
  - 2 x 32-bit instruction fetch and decode.
  - 2 x 32-bit I-cache and memory interface.
  - Upgrade to 64-bit paths in future version.

- 5-plus-1 Pipeline Architecture:
  - Q Stage, prediction for branches
  - Single Load Delay slot
  - Single Clock Edge design

MiniRISC CW4010 Overview (3)

- Power Management Features
  - Fully static design; gated clocks.
  - Wait for interrupt instruction.
  - Estimated core power consumption: 5mW/MHz.

- Full scan support included in core design
  - Simplifies device and board production test.
  - Supports ICE-like debug capability.
MiniRISC CW4010 Instruction Set

- Implements full MIPS-II instruction set
- Additional instructions
  - ffs, ffc: Find First Set Bit.
  - FP emulation and bit tests.
  - selsr, selsl: Select and shift.
  - Graphics alignment and bit field selection.
  - addciu: Add circular Immediate.
  - Circular Buffer addressing.
  - madd, msub: Multiply/Accumulate and Multiply/subtract.
  - DSP and graphics calculations.
  - waiti: Wait for Interrupt.
  - Power management feature.

MiniRISC CW4010 Internal Organization

- 4010 core contains basic Integer Unit
- 4010 shell contains optional blocks, memories
MiniRISC CW4010 Pipeline (1)

Basic 2-way superscalar machine
- Max. 2 fetches/decodes/issues/execs/writes per clock.

To issue a pair of instructions without stalling:
- Both instructions must use different execution units.
- Second instruction may not use result of first.
- Neither instruction may use result of any previously issued operation which is still incomplete.
- Special case: two adds or load-immediates can issue.
- Instructions stall at RD stage unless/until issued.

Execution behavior
- ALU instructions execute in-order, single cycle.
- Mul/Div instructions execute concurrently with ALU.
- Loads block only if target register used during latency.
MiniRISC CW4010 modular building blocks

- ICache/DCache Configuration
  - Direct Map / 2-way Set Associative
  - Options: 0, 1, 2, 4, or 8 K Bytes per set
- Write-back buffer
  - Removable for WriteThrough Cache Configuration
- MMU
  - Removable for non-MMU system
  - Selectable TLB Configuration (Size, Mask, etc)
- Multiplier
  - Options: None / Small / Fast with accumulate
  - Support Multiply/Add Instruction as an option

MiniRISC CW4010 MMU

- Memory Management Unit similar to R4000.
- Up to 64 single entry pages instead of 48 dual entry pages.
  - Eases MMU h/w design; simplifies memory mapping.
- Two page sizes (4K, 16M) instead of six.
- Write thru/write-back/none selectable per page.
- MMU may be removed if not required.
  - If omitted, single config bit sets write mode globally.
MiniRISC CW4010 Instruction Cache

- ICache 2KBytes to 16KBytes options (8K/set).
- Direct mapped or 2-way set associative.
- Block refill requests miss word first.
- Linear ordering; wraparound at end of block.
- Instruction Streaming.

MiniRISC CW4010 Data Cache

- DCache 0Kbytes to 16KBytes options (8K/set).
- Direct mapped or 2-way set associative.
- Early release of Data Cache.
- Single Load Miss does not stall CPU.
- Store hit under Load Miss.
MiniRISC CW4010 Interfaces

- On-chip bus Interface
  - Address[31:0]; Data[63:0]; ByteEnable[7:0]; Controls

- Coprocessor Interface
  - InstructionBus[31:0]; DataIn/Out[31:0]; Controls

- Cache Invalidation Interface
  - AddressInputs[31:5]; Invalidation Strobe
  - Allows connection of bus-snooping logic

MiniRISC CW4010 On-chip bus

- Basic transaction: 64b width, single clock cycle
  - Full CPU data rate available for onchip peripherals.
  - Off chip bus(es) may sacrifice speed, width.
  - One dead cycle inserted for any bus turnaround.

- Single (1, 2, 3, 4, 8 bytes) or Burst (8 words)
  - System can force idle cycles between transactions, or to break up bursts.

- Other features:
  - Bus Retry, Bus Error.
  - Atomic transactions (bus lock) for semaphores.
  - Dynamic sizing to 32bit.
  - In-page write signal for DRAM support.
**MiniRISC CW4010 Development Support**

- Uses standard or enhanced software tools
  - MIPS tools are available from many vendors.
  - Tools optimized for CW4010 in development.

- HDL Simulation and Verification Environment
  - Includes HDL model, timing shell, synthesis shell.
  - Ready-made framework for ASIC designs.
  - User defined blocks connect to this working nucleus.

- ICE-like debug tools
  - Use CW4010's internal scan chain.
  - Full control & observability of deeply embedded core.
  - Initial bringup of new device in system.
  - Hardware/Software integration, system level debug.

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**MiniRISC CW4010 Evaluation Chip**

Implemented in 0.5 um; 80MHz
MiniRISC CW4010 Performance

- Estimated performance
  - ~110 native MIPS sustained, on general purpose integer code.
  - 5mW/MHz core power consumption.

- With standard MIPS C software tools:
  - Average around 1.3 instructions per clock (over a group of small synthetic benchmarks).
  - 1.3 times R3000 / 33300 / 4200 at same clock rate.
  - 1.7 times R4400 at same clock rate.

- With CW4010-optimized C software tools:
  - Average 1.4 to 1.8 instructions per clock.