Hot Compilers for Future Hot Chips

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Microprocessor Directions

- Current trends
  - Higher clock rate
  - More instruction level parallelism (ILP)

- Alternate direction: Multiple superscalar processors on a chip
  - Hardware advantages over Very Wide superscalars:
    - Simpler, Faster
    - Less wires
    - Multiported caches → separate caches
    - Multiported registers → separate register files
    - Data dependence between instructions → disjoint sets
  - Software advantages:
    - Supports multiprogramming
    - Supports explicit parallel programming

- Key question: Performance of individual applications?
  Are multiprocessors competitive to processors with high ILP?
Potential Advantage of Multiprocessors

- High ILP → Wide variation of program performance
- Diminishing return of ILP
Challenges for Multiprocessor Compilers

- Programs with high ILP
  - Must minimize synchronization and communication cost

- Programs with low ILP
  - Multiprocessors' unique advantage →
    Extract independent threads of computation

- Programs written in C
  - Pointer analysis

SUIF Compiler Research Project

- SUIF (Stanford University Intermediate Format)

  • A fully functional compiler research infrastructure
  • Base version has been released and is freely available
  • Techniques described will be incorporated in future releases

- Techniques expected to be transferred to industry in a few years
I. Pointer Analysis

• Important for C code
  • To reorder/parallelize loads&stores through pointers

• Efficient and accurate analysis for
  • Parameter passing
  • Pointer assignments
  • Direct array address calculations (*p++)
  • Function pointers

• Technique: Interprocedural pointer analysis algorithm
  • Avoids re-analyzing a function
    by determining the relevant pointer aliases at call sites
  • [Wilson&Lam, ACM PLDI Conference ‘95]

• Future research
  • Efficient analysis of recursive data structures

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Preliminary Results

<table>
<thead>
<tr>
<th>Program</th>
<th>Lines</th>
<th>Procedures</th>
<th>Analysis Time DEC 5000 (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>alvinn</td>
<td>272</td>
<td>8</td>
<td>0.29</td>
</tr>
<tr>
<td>grep</td>
<td>430</td>
<td>9</td>
<td>0.57</td>
</tr>
<tr>
<td>diff</td>
<td>668</td>
<td>23</td>
<td>1.31</td>
</tr>
<tr>
<td>lex315</td>
<td>776</td>
<td>16</td>
<td>0.85</td>
</tr>
<tr>
<td>compress</td>
<td>1503</td>
<td>14</td>
<td>1.29</td>
</tr>
<tr>
<td>loader</td>
<td>1539</td>
<td>29</td>
<td>1.43</td>
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<td>football</td>
<td>2354</td>
<td>57</td>
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<tr>
<td>compiler</td>
<td>2360</td>
<td>37</td>
<td>5.86</td>
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<tr>
<td>assembler</td>
<td>3361</td>
<td>51</td>
<td>4.37</td>
</tr>
<tr>
<td>eqntott</td>
<td>3454</td>
<td>60</td>
<td>6.17</td>
</tr>
<tr>
<td>ear</td>
<td>4284</td>
<td>68</td>
<td>2.41</td>
</tr>
<tr>
<td>simulator</td>
<td>4663</td>
<td>98</td>
<td>9.89</td>
</tr>
</tbody>
</table>

• Can find all loop-level parallelism in both SPEC92fp C programs
II. Finding Coarse-Grain Parallelism

<table>
<thead>
<tr>
<th>First Generation Parallelizers</th>
<th>SUIF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optimizations on <em>scalar</em> variables</td>
<td>Optimizations on <em>array</em> variables</td>
</tr>
<tr>
<td><em>Within</em> procedures</td>
<td><em>Across</em> procedures</td>
</tr>
</tbody>
</table>

- **Reference**
  - [Hall et al., Supercomputer 95]

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**Reductions**

- **Generalized to reductions on (portions of) arrays**
  - in either dense or sparse representation
Privatization

• Each processor keeps a private copy of temporary data

Loop Iterations

A = A
= A

A = A
= A

A = A
= A

A = A
= A

A = A
= A

A = A
= A

A = A
= A

• Generalized to privatizing arrays
  • Requires data flow analysis on individual array elements

Interprocedural Analysis

• Algorithm
  • Based on interval analysis
  • Complexity: Analyze each function 3 times
  • Incremental compilation possible by saving summary information

• Important to have a complete suite of interprocedural analyses
  • Constant propagation
  • Loop invariant analysis
  • Induction variable analysis
  • Scalar privatization
  • Scalar reduction recognition
  • Array data dependence analysis
  • Array privatization
  • Reductions to regions of arrays
NAS Parallel Benchmarks on SGI Challenge

Improvement due to more parallelism:

![Graphs showing speedup vs. number of processors for cgmp and embar(APR)]

Improvement due to less frequent synchronization:

![Graphs showing speedup vs. number of processors for appbt and appsp]

6.1-14

Observations

- **Parallelizers are maturing**
  - Interprocedural analysis
  - Array reduction and privatization

- **An interactive parallelizer will be a useful tool**
III. Optimizations

- Minimize synchronization & cache traffic across loops
  - 1st generation parallelizers
    - Insert barriers between every parallel loop
    - Distribute iterations in each loop independently
  - New global analysis
    - Smart assignment of iterations to eliminate barriers and cache traffic

EXAMPLE: tomcatv

```
DO J = 
  DO I = (parallelizable) 
    RX(I,J) = ... - RX(I,J-1)
  I
J
```

```
DO L = (parallelizable) 
  DO I = (parallelizable) 
    ... = RX(I,L)
```

Data Restructuring

- Problem
  - False sharing: processors sharing same cache line but not data
  - Conflicts: set associativity maps data to same cache position

- Solution:
  - Make data accessed by each processor contiguous via data transposes and blocking
Stanford DASH Multiprocessors

- Characteristics
  - Directory-based, cache-coherent NUMA
  - 32 33MHz MIPS R3000 in 8 clusters
  - 64KB 1st level direct-mapped cache, 256KB 2nd level cache

- Techniques also useful for small-scale multiprocessors made out of fast processors

Experimental Results: Kernels

- LU 256x256
- ADI Integration 256x256
- 5 point stencil 512x512
- 1Kx1K
- Speedup vs. Number of Processors

Legend:
- ▲ SUIF
- △ 1st Generation Parallelizer
Programs

**Erlebacher**

![Graph for Erlebacher](image)

**Vpenta**

![Graph for Vpenta](image)

**SWM256**

![Graph for SWM256](image)

**Tomcatv**

![Graph for Tomcatv](image)

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6.1-20

**Results on SPEC92 fp**

... will be reported in the meeting
Conclusions

- Maturation of parallelizing compilers
  - Pointer analysis
  - Outer loop parallelism
  - Synchronization and cache optimizations
  - Interactive compilers will be effective in finding parallelism

- Build multiprocessors with superscalar processors instead of very wide superscalars
  - More cost-effective
  - More versatile
    - Thread and instruction level parallelism
    - Multiprogramming
  - Fine-grain parallelism possible with better support → multiprocessors on a chip