A 150MHz Superscalar RISC Processor with Pseudo Vector Processing Feature

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Presentation Outline

- Design Goals
- Pseudo Vector Processing Feature
- Processor Overview
- Performance
- Physical Characteristics
- Summary
Design Goals

- Competitive Performance
- Implementation of Pseudo Vector Processing Feature
- Effective High Memory Throughput
- 0.3µm CMOS Technology
- High Operating Frequency
- Low Power

Architectural Features

- Support for Uncacheable Memory Pages
- Pseudo Vector Processing Feature based on Slide-Windowed Registers (PVP-SW)
  - Utilize Software-Pipelining Technique
  - Flexible Software-Supported Register Renaming
- Architectural Extensions
  - Slide-Windowed Floating-Point Registers
  - Preload Instruction
  - Poststore Instruction
Slide-Windowed Floating-Point Registers

- Global registers - - - 8 or 12 or 16
- Window offset = FWSTP (Floating Window STart Pointer)
- FWSTPset instruction

Preload Instruction

- Directly specify 128 Physical FPRs
  - to hide Memory Access Latency
  - 7-bit register number
- Data Transfer from Main Memory to FPR directly
  - No Cache Pollution
- Preload 8B Data / cycle
  - 1.2GB/s Peak Transfer Rate @ 150MHz
- Compatibility with Cache

<table>
<thead>
<tr>
<th>1st cache</th>
<th>2nd cache</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>hit</td>
<td>don't care</td>
<td>1st cache -&gt; FPR</td>
</tr>
<tr>
<td>miss</td>
<td>don't care</td>
<td>M.M. -&gt; FPR</td>
</tr>
</tbody>
</table>
Poststore Instruction

- Directly specify 128 Physical FPRs
  - to hide FP Latency
  - 7-bit register number
- Compatibility with Cache
  - 1st or 2nd cache hit -> Cache Store and M.M. Store
  - 1st and 2nd cache miss -> M.M. Store only

Processor Core Features

- Superscalar with 2 Instruction Issues
- Up to 4 Operations / cycle
- 2 Integer ALUs, 2 SMUs (Shift Merge Unit)
- 2 Floating-point Operations (FMPADD) / cycle
- Branch History Table with 2-bit x 1024 Entries
TLB Organization

- 1st Level TLB
  
  I-TLB  256 Entries  direct mapped  
  6 Block Table Entries  512K-32MB/Entry  
  1 Anti-Thrashing Entry  

  D-TLB  256 Entries  direct mapped  
  6 Block Table Entries  512K-32MB/Entry  
  1 Anti-Thrashing Entry  

- 2nd Level TLB
  
  I-TLB  1K-4K Entries  2 way set associative  
  D-TLB  1K-4K Entries  2 way set associative
Cache Organization

- 1st Level Cache
  - I-Cache: 16KB
  - D-Cache: 16KB
  - Direct Mapped, 32B / Block
  - Single Bit Error Detection Parity

- 2nd Level Cache
  - I/D Combined: 512KB-8MB
  - Direct Mapped, 128B / Line
  - Single Bit Error Correction, Double bits Error Detection ECC / 4B

- Cache Miss Optimization
  - Hit under Miss
  - Pipelined Instruction Prefetching (up to 4)

Integer Pipeline: 6 stages

<table>
<thead>
<tr>
<th>IF</th>
<th>D</th>
<th>E</th>
<th>A</th>
<th>N</th>
<th>W</th>
</tr>
</thead>
</table>

Bypass

IF: Instruction Fetch
D: Decode
E: Execution
A: Cache/TLB Access
N: Nullification / Interruption
W: GR Write

Floating Pipeline: 7 stages

<table>
<thead>
<tr>
<th>IF</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>E1</th>
<th>E2</th>
<th>Z</th>
</tr>
</thead>
</table>

Bypass

D1: FPR Number Conversion
D2: Dependency Check
D3: Source Operand Read
E1: Execution 1
E2: Execution 2
Z: FPR Write
### FP Latency and Issue Rate

<table>
<thead>
<tr>
<th></th>
<th>Single Precision</th>
<th>Double Precision</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Latency / Issue Rate</td>
<td>Latency / Issue Rate</td>
</tr>
<tr>
<td>Add, Sub</td>
<td>2 / 1</td>
<td>2 / 1</td>
</tr>
<tr>
<td>Multiply</td>
<td>2 / 1</td>
<td>2 / 1</td>
</tr>
<tr>
<td>FMPYADD, FMPYSUB</td>
<td>2 / 1</td>
<td>2 / 1</td>
</tr>
<tr>
<td>Divide</td>
<td>10 / 9</td>
<td>17 / 16</td>
</tr>
<tr>
<td>Square Root</td>
<td>16 / 15</td>
<td>30 / 29</td>
</tr>
</tbody>
</table>

### Performance

Loop Performance of Pseudo Vector Processing Feature (PVP-SW)

\[
\text{do 10 } K = 1,N \\
\text{10 } S = S + A(K) * B(K)
\]

- 1st Cache Hit
- 1st Cache Miss
- 2nd Cache Hit
- 2nd Cache Miss

- **With PVP-SW**
- **Without PVP-SW**
Physical Characteristics

Process Technology 0.3 \( \mu \text{m} \) CMOS
Cycle Time 150 MHz (*1)
> 200 MHz (*2)
Die Size 15.7 mm x 15.7 mm
Number of Transistors 4.5 M
Package 1672 pin CCB (C4), 520 signals
Power Supply 2.5 V
Power Dissipation 13 W @ 150 MHz
Peak MFLOPS / W 23 MFLOPS / W

(*1) Worst Silicon Processing and Worst Environment
(*2) Typical Silicon Processing and Worst Environment

Device Characteristics

• CMOS Circuit
  
  L\text{drawn} \quad 0.3 \mu \text{m}
  
  L\text{eff} \quad 0.25 \mu \text{m}
  
  Tox \quad 6.5 \text{ nm}

• Interconnection
  
  Layers 4 Metal layers
  
  \begin{tabular}{|c|c|c|c|c|}
  \hline
  Width (\mu m) & Thickness (\mu m) & Pitch (\mu m) & \\
  & & Uncontacted & Contacted & Design Rule \\
  \hline
  AL1 & 0.5 & 0.65 & 1.0 & 1.4 & 1.4 \\
  AL2 & 0.5 & 0.65 & 1.0 & 1.4 & 1.4 \\
  AL3 & 1.4 & 1.15 & 1.8 & 2.4 & 2.8 \\
  AL4 & 1.4 & 1.45 & 2.8 & 2.8 & 2.8 \\
  \hline
  \end{tabular}
Summary

- High Performance Superscalar RISC Processor
- PVP-SW Feature Support
- Optimized to Large Scale Scientific Calculations
- High Memory Throughput
- High Clock Frequency