Smaller, Faster, Cooler...
Evolving The PowerPC Family

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Agenda

- PowerPC ISA
- 1995 Commitments
- Design Methodology
- Portable Design Characteristics
- 603ev Design Point
  - Design features
  - Block diagram
  - Instruction pipeline / latencies
  - Technology
  - Specifications
  - Competitiveness
Instruction Set Architecture

- Jointly Derived by IBM / Apple / Motorola
- Maintained The ABI With POWER
- Simplify Architecture
  - More appropriate for low-cost single chip microprocessors
- Eliminate Instructions That Impede Clock Rates
- Remove Architecturally Imposed Barrier To:
  - Superscalar dispatch
  - Out-of-order execution
- New Features
  - Multi-processing support
  - Extension to 64 bits
  - Bi-endian support

1995 Commitments

- 620 Family
  - 330 SPECint 92
  - 410 SPECfp 92

- 604 Family
  - 225 SPECint 92
  - 250 SPECfp 92

- 601 Family
  - 125 SPECint 92
  - 150 SPECfp 92

- 603 Family
  - 160 SPECint 92
  - 140 SPECfp 92

- 602 Family
  - 50 SPECint
  - 125K Dhrystones

*estimated performance
Design Methodology

Somerset Design Methodology

- Early performance trade-offs
- Early implementation decisions
- High throughput, W5 based
- Efficient vector generation
- Efficient logic design
- Timing, Test, Functional, & Physical
- Gate level: Functional level
- RC and Wiring estimators
- Identifies all paths on chip
- RC extraction from wiring
- Short circuit run times
- Short test development time

Goal:
First Pass Silicon Functionality, at frequency, and on time

Arrays - Tags, TLB, BTAC, Etc..
PLL - Phase Lock Loop
COP - Common On Chip Processor
   » JTAG
   » LSSD Control
RLM - Random Logic Macro
   » Control Logic
Super macro - Collection of Custom, RLM, Wiring Cells
LST - Logic Service Terminal
Design Methodology

- Overall Design Objective
  - 1st pass silicon functionality at performance
  - Design on schedule
- Flexible Design Methodology
  - Vary degree of customization to meet schedule/performance objectives
  - Early design performance trade-off's
  - Early cycle time determination (estimated values)
  - Early floor planning
- Building Block Approach
  - Standard cells for control logic (book)
  - Custom-off-the-shelf data flow macros (ots)
  - Full custom arrays and cycle time critical circuits (custom ots)
- Rules Based
- Two Primary Views of Chip
  - Logical
  - Physical

Design Methodology

- Floorplanning/Chip Construction
  - Rule based
  - Hierarchical
  - RC estimates for timing
    » early timing estimates
    » based on real physical constraints
    » refined as design progresses
  - Pre-wires for critical areas
  - Auto-route program incorporates pre-wires
- Static Timing Analysis
  - All possible chip paths analyzed
  - Report of path slacks from target cycle time
- Design For Test
  - Level sensitive scan design (LSSD)
  - Automatic test pattern generation (ATPG)
  - Built in self-test (BIST)
Portable Design Characteristics

- Aggressive Performance
  - lags the desktop by 12 mths

- Low Power
  - under 3 watts

- Cost Sensitive
  - under 100 mm²

- Versatile
  - wide range of system configurations

Design Features

- Increased Cache Size Over PPC603
- Support For Non-integer Bus Clock Multiples
- 5 Volt Tolerant I/O
- Unaligned Little Endian Support
- Hit Under Miss On I-cache
- Improved Divide Performance
- Simplified Memory Addressing (No PIO)
- Power Management
- Improved Clocking
Block Diagram

Instruction Pipeline
- Dynamic Power Management
  - Inactive units are not clocked

- Static Power Management:
  - Doze: timers, snooping only
  - Nap: timers only
  - Sleep: no clocks
Process Technology

- 0.5u Nwell CMOS
- Five Level Metal
- Local Interconnect
- $L_{\text{eff}} = 0.25\mu m$
- 2.5v Core Voltage
- 3.3v Receivers / Drivers

Specifications

- Superscalar Low Power RISC Processor
- 16K Instruction Cache, 16K Data Cache
- 165 SPECint92 at 167 MHz \((\text{estimated})\)
- 81 sq mm. Die Size
- 2.6 Million Transistors
- 2.5w Typical Power at 167 MHz \((\text{estimated})\)
- 165 I/O Signals, CMOS/TTL Compatible
- LSSD Design, JTAG Compliant
- Quad Flat Pack & Ball Grid Array Packages
Competitiveness

Die Size (mm²)

Power (watts)

Performance (SPECint92)

Processor Performance/(Power*Size)

IBM

Apple

7.3-18

Competitiveness
603ev Processor

- Fully Functional First Pass Silicon
- Rapid Market Introduction
  - highly compatible design
  - samples in 4Q95, production in 1Q96
- High Performance
  - 165 SPECint92, 150 SPECfp92 (estimated)
- Low Power
  - 2.5w typical (estimated)
  - doze / nap / sleep power saving modes
- Low Cost
  - small die size
  - proven technology