R10000 Superscalar Microprocessor


Presentation Outline

- Architecture of CPU and FPU
- Memory Hierarchy
- System Configuration
- Verification and Design Methods
**R10000 - Block Diagram**

- Refill (4 words/cycle)
- Instr. Pre-Decode
- Istr. Cache
- Instr. Decode Branch
- Branch Address
- 32K-bytes 2-way associative
  4 instr./cycle 4 instr./cycle
- Register Rename
- Map Tables
- Active List
- Free Lists
- 4 instr./cycle 16 entries
- FltPt. Register File 64x64 bits
- FltPt. Queue
- Integer Register File 64x64 bits
- Integer Queue
- 16 entries
- Integer ALU
- Integer ALU
- Integer ALU
- Load / Store
- (Translation Look-aside Buffer) 64 dual entries.
- Two Arithmetic/Logic Units
- Integer Calculate
- Integer ALU
- Integer ALU
- Integer Register Operands
- Integer Register Operands
- 2-way Interleaved Cache
- TLB
- FltPt. Adder
- FltPt. Multiplier
- Divisor, Sqrt
- Sec. Cache
- System Interface Logic
- Refill / Copyback
- Instruction Fetch and Decode
- Functional Units (Execute Instruction)

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**R10000 - Pipelines**

- Stage 1
- Stage 2
- Stage 3
- Stage 4
- Stage 5
- Stage 6
- Stage 7
- Branch Addresses
  - Branch Pred
  - Branch Unit
  - Instr. Cache
  - Decode
  - Map
  - Busy
  - Register Renaming

- Floating-Point Add Pipeline
- FltPt. Multiply Pipeline
- Integer Pipeline
- Integer Pipeline
- Load/Store Pipeline

- Floating-Point Queue and Registers
- Integer Register Operands
- Integer Register Operands
- 2-way Interleaved Cache
- Translation Look-aside Buffer

- Instruction Fetch, Decode and Map Pipeline (4 instructions/cycle)

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**Register Renaming**

Original Instruction Format (in memory)

Instruction is re-arranged during instruction predecode. Example shows a simple integer ALU instruction, such as an ADD.

Instruction Format in Instruction Cache

Update Mapping Table

12 Read Ports

Integer Mapping Table 32-word by 6-bit RAM

Integer Free List 32-word by 6-bit RAM

Return to Free List when instruction graduates.

During any cycle, each physical register number is either in Mapping Table, Active List, or Free List.

**Control Paths**

Fetch and Decode 4 Instructions per cycle

Register Renaming 6-bit Control Logic

Five Execution Units 64-bit Data Path

Fetch and Decode

4 Instructions per cycle

op rs rt rd fn

"Logical" registers

"Physical" registers

Queue

Int/Flt Map Table

32x6-bit

Int Q

Addr Q

Flt Q

Active List

Free List

List of unused registers.

No reservation stations or re-ordering buffers.

Operands are bypassed or read directly from Register File. Results are written directly back into Register File.

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**Instruction Fetch and Branch**

Fetch, align, and decode four instructions in parallel.

- **Sec. Cache** 4x32
- **Pre-Decide**
- **Refill** Append 4-bit unit code.
- **2-way set-associative**
- **Main TLB** Refill
- **Instr TLB**
- **64 entries**
- **Branch History**
- **512 x 2-bit**
- **Instr. Fetch Virtual Address**

**Branch Unit**

- **Branch Instr. Register**
- **Br. Address**
- **4 entries**
- **Branch Stack**
- **4 instr. to Queues**

**Floating-Point Units**

CSA = Carry Save Adder
CPA = Carry Propagate Adder
LZP = Leading Zero Predict

- **Floating-Point Register File (54 x 64-bits)**
  - Read
  - Unpack
  - 3 Cycle Bypass
  - 3 Cycle Bypass
  - Compression Tree using (4,2) CSA's
  - 106-bit CPA
  - Round
  - 54-bit CPA
  - MULTIPLIER
  - Iterative Units
  - ADDER
  - Fully Pipelined Units

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**R10000 Memory Hierarchy**

- **CPU**
  - Doubleword Load/Store
  - On-chip Primary Caches
  - Quadword Refill/Write-back
  - External Secondary Cache
  - Main Memory

- **Instruction Fetch**
- **R10000 Processor**
- **Load/Store Unit**

- **4 Instructions**
  - Stream
  - Load
  - Store

- **52KB**
  - Tag0
  - Tag1
  - Way 0
  - Way 1
  - Instr. Cache

- **16KB**
  - Tag0
  - Tag1
  - Way 0
  - Way 1
  - Bank 0
  - Bank 1
  - Data Cache

- **512KB to 16MB**

- **External Agent**
- **Main Memory**

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**Parallelism in Data Cache**

- **Address[5] = 0**
  - **Bank 0**
  - Cache Tag: 512-word by 32-bit RAM
  - Cache Data: 2048-word by 64-bit RAM

- **Address[5] = 1**
  - **Bank 1**
  - Cache Tag: 512-word by 32-bit RAM
  - Cache Data: 2048-word by 64-bit RAM

- **Adr Queue**
  - ADDR CALC: 44-bit Adder
  - TAG CHECK: Is block in cache?
  - LOAD UNIT: Load integer or Fl, Fp
  - STORE UNIT: Store integer or Fl, Fp

- **Ext Interface**
  - Refill, Write-Back
  - Interrogate, Invalidate

- Instruction which calculates address may also use tag compare and load in parallel.

- Four sections can be independently allocated.
- CPU accesses are 64 bits wide, 2-way associative.
- Refill and write-back are 128 bits wide. (Way is known.)

- Highest priority for any section.
  - Refills 8-word block in two cycles.
  - Writes back dirty blocks in two cycles.

- Initiates refill.
  - Load may be completed later.
Data Cache Pipelines

Load which hits in primary cache:
Cycle 1. Issue Queue
Cycle 2. Addr Calc
Cycle 3. TLB
  Tag Check
  Data Load
  Address Calculate/Translation Pipeline
  Tag Check Pipeline
  Data Load Pipeline
Instruction is "done", but it must wait in Address Queue until Graduation.

Store which hits in primary cache:
Cycle 1. Issue Queue
Cycle 2. Addr Calc
Cycle 3. TLB
  Tag Check
  Store
  Data Store Pipeline
Two banks reduce conflict for resources.
Retry operations, which already know address, arbitrate resources.
Wait for Graduation.

Load which misses in primary cache:
Cycle 1. Issue Queue
Cycle 2. Addr Calc
Cycle 3. TLB
  Tag Check
  Data Load
  Address
  RAM Access
  Data Transfer
  First of 2 cycles 4 words/cycle
Primary Cache Miss initiates refill from secondary cache.

Non-blocking Cache

Cycles Per Instr (CPI): Concurrent refill times reduce effective cache latency.
Simulated results
Spec Benchmarks:
SC
Spread Sheet 1.08
0.83
0.25
+16% Extra time with blocking cache.
compress
File Compression 1.37
0.65
0.72
+19%
fpripp
Quantum Chemistry 0.70
0.69
(Fits in primary cache.)
doduc
Thermal-hydraulic Model 1.03
0.87
0.16
+13%
ora
Spherical Ray Tracing (Reciprocal, Sqr Roots) 1.74
1.74
0%
(Fits in primary.)
tomcatv
Vector Fit-Pt 1.37
0.74
0.62
+47%
0.93
Total Miss Latencies
CPI without overlap Actual R10000 CPI
Perfect Cache Effective Miss Latency
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Data Cache Interleaving

Bank 0
Array 0
Way 0
Way 1
Way 0
Way 1
Set 0
Set 0
CPU accesses one doubleword. Simultaneous tag check selects way.

Array 1
Way 0
Way 1
Way 0
Way 1

Bank 1
Array 0
Way 0
Way 1
Way 0
Way 1
Set 1
Set 1
External Interface accesses quadword as two doublewords in parallel.

Array 1
Way 0
Way 1
Way 0
Way 1

Quadword (Way is known early.)

Doubleword 0
Doubleword 1
Doubleword 2
Doubleword 3

System Configurations

Secondary Cache
512K to 16M byte SSRAM
2-way set associative

Secondary Cache interface
- 19 bit replicated address bus
- 26-bit tag bus with 7-bit ECC
- 128-bit data bus with 9-bit ECC
- Clock Dividers 1, 1.5, 2, 2.5, 3 supported

1 to 4 processors

R10000

Duplicate Tags
External Agent

Directory

System Interface Bus
- 3 arbitration signals
- 2 flow control signals
- 12-bit command bus with parity
- 64-bit mixed adra/data bus with 8-bit ECC
- 3-bit processor state response bus with parity
- 5-bit external response bus with parity
- Clock Dividers 1, 1.5, 2, 2.5, 3, 3.5, 4 supported
Clocks and Output Drivers

LV-CMOS or HSTL-1 tristate or HSTL-2 open drain

System Interface

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Align Edges

Internal Clocks

CPU etc.

Data

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Address

2 * 19

SSRAM

(Ten parts)

Secondary Cache

RAM Array

6 differential

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Refill from Set-Associative Secondary Cache

Primary Cache

Miss

MRU Table

Read 8192-bit "Most Recently Used" Table (MRU). MRU way is read first, because it is likely to be needed.

SRAM Index

Addr

Addr

SRAM Read

RAM

RAM

RAM

RAM

128-bit Data

A0

A1

B0

B1

Address Tag

A

B

Secondary Cache Tag Check

Tags in both ways are read sequentially.

Hit in Secondary Cache?

Refill secondary cache if both A and B miss.

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**Secondary Cache Error Protection**

- **Parity**
- **Data**
- **ECC bits**

Fast Logic Path:
- Parity Error (odd-bit) Inhibit loading of bad data
- Normal low-latency path

Primary Refill Data:

Caches:
- Single-bit error (correction)
- Multi-bit error (exception)

Pad Ring 2-cycle Correction Pipeline

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**System Interface Block Diagram**

From Secondary Cache 36 128
- Outgoing Buffer 5 x 8 x 128
- Cached Buffer
- ECC Generator

From Load/Store Unit 64
- Uncached Buffer 2 x 16 x 64

To Primary Caches 128 36
- Incoming Buffer 4 x 8 x 128
- Cluster Buffer
- ECC Checker/Corrector

System Interface Bus 64
**Functional Verification Methodology**

- Tools and environment:
  - Inhouse HDL and simulator with backup and replay.
  - Graphical user interface for simulation and regression.
  - An instruction level simulator as a reference machine, which checks
    - Architecture registers
    - Memory hierarchy
  - Programmable random code generators for UP and MP.
  - Arc coverage and consistency checking for state machines.
- C-based System Model supports
  - Secondary cache array, memory controller and array, bus controller.
  - Bus protocol checking.
  - External events:
    - programmable or purely random
    - imbeded in diagnostics for fine-grain control
  - 1 to 4 processor configuration.

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**Diagnostic Development**

- Directed Diagnostics
  - Architecture Verification Programs (AVP)
  - Microarchitecture Verification Programs (MVP)
  - Implementation Verification Programs (IVP)
- Random Diagnostics From Programmable Random Code Generators
  - Functional unit intensive
  - Load/Store intensive
  - Branch intensive
  - Mix of the above under UP and MP environments
- Diags are self-checking and/or compared with the reference machine.
- UP and MP applications.
- Booting O/S's on R10000 RTL : 2 Unix O/S's and NT.
Test Features

- On-chip virtual output pins:
  - Physical design partitioning
  - Direct observability of internal signals
  - Signature compression through LFSRs
    (Linear-Feedback Shift Register)

- Dedicated test structures:
  - No performance impact
  - No logic design overhead
  - No special clock requirements

- Enhanced debug and diagnostics:
  - Cycle-by-cycle sampling of internal signals
  - Observed signals correlate to logic specification
  - Signature analysis

- Test cost reduction:
  - No special ATE requirements
  - Internal test-output compression by signature
  - Test and fault partitioning
  - Reduced test time and higher fault coverage

Clock and Power Distribution

- Power / Ground (metal 4)
- Clock Generator
- Phase Lock Loop (Isolated at edge of chip)
- Double-frequency clock
- Global Clock Driver (at center of chip)
- Balanced Clock Tree (metal 4 with metal 3 shield)
- Area Clock Buffers
- Local Clock Buffers
Signal Repeaters on Long Wires

Distribution of long wires after repeaters inserted.
(Longest wires were broken into shorter segments.)

Original distribution of long wires.

R10000 Die Photo

This sheet shows physical placement of major blocks.
(Full color photo slide will be shown at Hot Chips.)