High Performance Caches: 
The Quiet Revolution

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FSRAM Division
Memory and Microprocessor Technology Group
Motorola Semiconductor Products Sector
Austin, Texas
Intel Processor Core Clock Frequencies

Source: Intel Microprocessor Quick Reference Guide
Processor Core Speed Trends
The Long View

Source: Intel Microprocessor Quick Reference Guide
Processor Core Speed Trends

Source: Intel Microprocessor Quick Reference Guide
Intel System Bus Speeds

Year

Bus Freq. (MHz)

Source: Intel Microprocessor Quick Reference Guide
Volume Processor Max. Bus Speed Trend

Source: Intel Microprocessor Quick Reference Guide
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Cache SRAM Breakthroughs

- 300 MHz Barrier
  Echo Clock Conversion

- 150 MHz Barrier
  BGA Conversion

- 100 MHz Barrier
  Revo Conversion

- 50 MHz Barrier
  Sync Conversion

- Revolutionary Pinout
  Double Data FSRAM
  (Burst + Late Write)

- Revolutionary Pinout
  Burst Sync FSRAM

- Evolutionary Pinout
  Async FSRAM

- Evolutionary Pinout
  Burst Sync FSRAM

- Evolutionary Pinout
  Async FSRAM
Evolutionary
Pinout and Architecture
FSRAM

Revolutionary
Pinout and Architecture
FSRAM

Note: Drawings not to scale
Asynchronous Read-Write Sequence

Address

Select

Write

Data
Evolutionary
Pinout and Architecture
 Pipelined Burst SRAM

x16 PLCC

x32 TQFP

Note: Drawings not to scale
Pipelined Burst Synchronous Read-Write-Read Sequence

Clock

Address

Control

Data

T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11

0 n/a n/a 1 2

Read NoOp NoOp Write Read

0 1 2
Pipelined Synchronous BurstRAM Burst Read Sequence

Clock

Address

Control

Data

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- 300 MHz Barrier Echo Clock Conversion
- 150 MHz Barrier BGA Conversion
- 100 MHz Barrier Revo Conversion
- 50 MHz Barrier Sync Conversion
- Revolutionary Pinout Async FSRAM
- Revolutionary Pinout Sync Late Write FSRAM
- Revolutionary Pinout Burst Sync FSRAM
- Revolutionary Pinout Double Data FSRAM (Burst + Late Write)
Processor Core Frequency vs. Volume Bus Frequency

Date

Core Freq. / Bus Freq

Volume uP
High End uP

MOTOROLA
**Back Side L2 Port Architecture**

Frees FSRAMs to Run at Core Frequency

- The **Traditional** CPU/ L2 Cache Architecture
  - Processor Bus Speed constrained by load to
    - 100 MHz - 133MHz in Workstation Market
    - 50 MHz - 66MHz in the PC Market
  - L2 Cache sits on the slow processor bus

- The **Emerging** CPU/ L2 Cache Architecture
  - Processor Bus Speed constrained by load to
    - 100 MHz - 133MHz in Workstation Market
    - 50 MHz - 66MHz in the PC Market
  - Cache Bus Speed
    - 133 MHz - 250 MHz in Workstation Market
    - 90 MHz - 133 MHz in the PC Market
Revolutionary Pinout and Architecture
Late Write SRAM
in Plastic BGA Package

Bottom View

Top View

Note: Drawings not to scale
R/R Late Write Synchronous Read-Write-Read Sequence

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- Async
- Revo Async BurstRAM
- LW RAM
- DDR RAM
Cache SRAM Breakthroughs

- 300 MHz Barrier
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  Sync Conversion

- Rev. Pinout
  Double Data FSRAM
  (Burst + Late Write)

- Rev. Pinout
  Burst Sync FSRAM

- Rev. Pinout
  Sync Late Write FSRAM

- Rev. Pinout
  Async FSRAM

- Ev. Pinout
  Async FSRAM

- Ev. Pinout
  Burst Sync FSRAM
Double Data Rate Synchronous FSRAM

1M thru 16M, x16/18/32/36
in 9x17 bump BGA, 50mil Pitch

1M thru 16M
x16, 18, 32, 36
Burst Sync
1.27mm Pitch
14mm x22mm Body
PBGA Package
HSTL I/O

Top View
Rev. 3.2 - 5/30/96

Key
DQ* = NC for x16/18 version
CQ* = NC on x16/18 version
SA* = NC for x32/36 version
DQ% and DQ*% = NC for x16/x32 version

Density Upgrades

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Double Data Burst Synchronous Read-Write-Read Sequence

Clock

Address

Control

Data

Echo

Clock

Double Data Burst Synchronous Read-Write-Read Sequence
L2 FSRAM Architectural Convergence

- BGA DDR RAM x18/x36
- BGA DDR RAM x32/x64
- BGA
- DDR RAM x18/x36 LW RAM
- BGA x18/x36 Pipe Burst
- TQFP x36 Pipe Burst
- TQFP x32 Pipe Burst
- PLCC x18 Pipe Burst
- PLCC x18 FT Burst
- TQFP x32 Pipe Burst

Year

66

100

133

166

200

250

300

350

400

450

500

94 95 96 97 98
The Quiet Revolution

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Echo Clock Conversion

150 MHz Barrier
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Revolutionary
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Double Data FSRAM
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Pinout
Burst Sync FSRAM

50 MHz Barrier
Sync Conversion

Evolutionary
Pinout
Async FSRAM

Evolutionary
Pinout
Burst Sync
FSRAM