P55C Micro-Architecture –
The First Implementation of the
MMX™ Technology

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August 20, 1996
Outline

● Micro Architecture Overview
  – Instruction Decode
  – Pairing
  – MMX™ Technology Execution Units
  – Pipeline

● Performance

● Summary
Implementation Goals and Challenges

- Significant performance improvement of multimedia and communications applications
- No impact on device speed
- Maximize usage of existing micro-architecture
  - New instructions to decode
  - Unique execution units
MMX™ Technology Implementation

MMX™ Technology Added in Parallel to the Existing Integer and FP H/W
Decoding MMX™ Technology Instructions

- 0F prefix becomes a mainstream opcode
  - All MMX™ technology instructions start with 0F
- Length decoder extended to 4 bytes
  - Quadruple 0F decode bandwidth
- Capable of issuing two MMX technology instructions per cycle

Decoder Supports Full Bandwidth for New Instructions
**MMX™ Technology**

**Execution Pipe**

- MMX™ technology instructions use the integer pipe
- After the Execute stage the MMX technology pipe continues to the Mex and WM stage
  - Multiply instructions continue in the MMX technology pipe to the M2, M3 and WMul stages
## MMX™ Technology Execution Units

- All MMX™ technology Instructions can be issued every clock

<table>
<thead>
<tr>
<th>Operation</th>
<th># Of Units</th>
<th>Latency</th>
<th>Throughput</th>
<th>Pipes</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALU</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>U and V</td>
</tr>
<tr>
<td>Multiplier</td>
<td>1</td>
<td>3</td>
<td>1</td>
<td>U or V</td>
</tr>
<tr>
<td>Shift/Pack/Unpack</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>U or V</td>
</tr>
<tr>
<td>Memory Access</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>U</td>
</tr>
<tr>
<td>Integer Register Access</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>U</td>
</tr>
</tbody>
</table>

Maximum Throughput for New Instructions
Most Instructions Can Be Paired
MMX™ Technology
Instructions Execution

IDCT Inner Loop Execution

Movq mm4, [edi]    /* load 1st 4 values
Movq mm7, [edx]    /* load 2nd 4 values
Movq mm0, mm4      /* Copy 1st values
Psubw mm4, mm7     /* O1[0-3] = I0[0-3] - I1[0-3]
Paddw mm7, mm0     /* O0[0-3] = I0[0-3] + I1[0-3]

Utilize SIMD and Micro-Architecture Parallelism
To Achieve Performance
P55C Multimedia Kernels Performance

- Complex FIR
- Complex FFT
- Inverse DCT
- Motion estimation
- Lag search
- Analysis filter

Categories:
- DSP
- Video
- Voice
Summary

- P55C with MMX™ technology will provide significant performance improvement for multimedia and communications applications
- Clean MMX technology implementation without sacrificing device speed
- P55C maximizes usage of existing Pentium® Processor micro-architecture
- Product introduction expected in Q1’97

Intel’s MMX technology -- For the next generation of multimedia and communications