Custom VLSI
for the
Compositing DAC
of the
Touchstone Multimedia Accelerator
Introduction

• Compositing DAC (C-DAC)
  • One of five related ASIC Components
  • Advanced Multimedia Architecture
  • Hot Chips Code Name: Touchstone
Touchstone Multimedia Architecture

Compositing
DAC

PCI Bus
MSP

POP

2 x 2M x 8 RDRAM

ILC

C-DAC

Media Bus

RGB Video

1394
USB

2 Ch Audio

Modem

Audio Bus

Audio

Media IO
C-DAC Chip Contribution

♦ Touchstone Function and Performance
  • 1344 x 1024 @ 75Hz
  • 24 bit true color at all resolutions
  • Optimized 3D Animation at 75 Hz - Combination of Image Layer Animation and 3D Rendering
  • Scene Complexity of >20,000 Rendered Polygons
  • Very High Image Quality - anisotropic filtering, subpixel anti-aliasing, shadows, reflections, etc.

♦ Cost Goals
  • PCI Add-in Card for Less Than $250 BOM Cost
  • Compositing DAC Targeted Cost < $35
**Touchstone Compositing DAC**

- Specialized Memory & Logic Device
- Alpha Compositing of Sprite Data
- Double Buffered Scanlines at 1344 x 32
- Processes 4 Pixels @ 32bpp @ 80MHz
- Compositing Rate: 320MPixels/sec
- Integrated DAC
- Standard RGB Output with Stereo

Diagram:

- 4 x 8 Sprite Alpha Data
- 4 x 24 Sprite Pixel RGB Data
- Media Bus
- RGB Video
- C-DAC
Compositing DAC Vital Statistics

- Package: SQFP
- # Pins: 304
- Power: 2.5 W
- Logic Transistors: ~ 350K
- Memory Transistors: ~ 15M
- Process Technology: 0.35 Micron C-MOS
C-DAC Challenges

♦ Potpourri of Circuitry
  • Logic, Memory, and Analog

♦ Price Point
  • SRAM based initial design to minimize risk
  • Rapid DRAM evolution required to meet consumer product cost goals

♦ Schedule
  • First Engineering Samples in 12 months
Compositing Buffer and DAC

- **Alpha Buffer**: 1360 x 32 x 8
- **Compositing Logic**
- **Scanline Buffer**: 1360 x 32 x 24 bits of RGB
- **Memory Control**
- **MUX**
- **Color LUT**: 256 x 8
- **DAC Output**
- **From Sprite Engine**
- **From Media DSP**
- **Media Bus Interface**
- **Clock Generator**
- **CRT Controller**
- **System Clocks**
- **HSync, VSync**

Four pixels per clock cycle.
Compositing DAC - Five Major Blocks

1. Compositing Engine
2. Compositing (Color and Beta) Buffers
3. 135 MHz LUT-DAC
4. 16-bit Media Bus Interface
5. CRT Controller & Clock Generator
Compositing Engine Logic

8 Bits each
Sprite Engine
RGB Data

Cursor
Mode

Sprite Engine
Alpha Data

Color
Compositor

Buffer
Multiplexer

Buffer Select

RGB - Buffer M

RGB - Buffer N

Pixel Valid

Beta Data

Beta Compositor

8 Bits each
Sprite Engine
RGB Data
Compositor Logic

1. Normal Mode

The Compositor Logic Performs the functions:

\[ C = B + B_{BETA} \times A \]
\[ C_{BETA} = B_{BETA} \times (1 - A_{ALPHA}) \]
- or -
\[ C_{BETA} = B_{BETA} \times A_{BETA} \]
Compositor Logic

2. Cursor Mode

- Incoming pixel is a cursor pixel.
- XORed with stored data to produce a cursor
- Stored alpha is unaltered

The equation is:

If A_ALPHA = 0x01,

\[
C = \text{NOT}(B) \\
C_{\text{BETA}} = B_{\text{BETA}}
\]

ELSE

\[
C = B + B_{\text{BETA}} \times A \\
C_{\text{BETA}} = B_{\text{BETA}} \times A_{\text{BETA}}
\]

END IF
Compositor Logic

where:

\[ A \] = Color of Incoming Pixel (From Sprite Engine)

\[ A_{\text{ALPHA}} \] = Coverage (Alpha) of Incoming Pixel

(from Sprite Engine)

\[ B \] = Stored Color (from Buffer)

\[ B_{\text{BETA}} \] = Stored Transparency

(Beta from Buffer: Beta = 1 - Alpha)

\[ C \] = Resultant Pixel Color

(new value to write back into buffer)

\[ C_{\text{BETA}} \] = Resultant Pixel Transparency

(New Beta to write back into buffer: Beta = 1 - Alpha)
**Color Composition Logic**

- One Pixel, One Channel
- Repeat 12 Times - 4 Pixels, 3 Channels
Beta Composition Logic

• One Pixel, One Channel

• Repeat 4 Times - for 4 Pixels
**Color Buffers**

Ping-pong buffers for each of the 8-bit RGB Channels

- Compositing in one of the Color Buffers
- Scanline-based read out of the other

- Two separate 10752 x 32-bit Dual Ported RAM arrays
  - Three instances of the Color Buffer for RGB

- Two 10752 x 1-bit Dual Ported RAM arrays for Pixel Valid

- Arrays contain a read port and a write port
  - Separate addresses generated for each port

- **Self refresh**

Challenge:
- Send pixels in an uninterrupted fashion to display
- Up to 1344 sequential row pixels MUST be read out at pixel clock
Color Buffer Implementation

WR_RED(31:00) -> 10752 x 32 RAM Array -> RD_RED(31:00)
WR_ADDR(13:00) -> RD_ADDR(13:00)
WR_GREEN(31:00) -> 10752 x 32 RAM Array -> RD_GREEN(31:00)
WR_BLUE(31:00) -> 10752 x 32 RAM Array -> RD_BLUE(31:00)
WR_PV -> 10752 x 32 RAM Array -> RD_PV
**Beta Buffer**

- One 10752 x 32-bit Dual Ported RAM Array
- Self refresh
- Accessed Only during compositing
  - Single-buffered
Beta Buffer Implementation

WR_ALPHA(31:00)  
WR_ADDR(13:00)  
WR

10752 x 32 RAM Array

RD_ALPHA(31:00)  
RD_ADDR(13:00)
Display & Compositor Addressing

Display Address Generator Logic

- Counters for row position and line position
- Circuitry for supporting the Line Sequential Stereo Mode
- Sprite Engine draws the left image in the stereo pair in the left half of the Compositing Buffer (LPC Count starting at pixel 0)
- Right image in the stereo pair in the right half of the Compositing Buffer (LPC Count starting at pixel 672)

• Compositor Address Generator
  - Receives the compositor address from the Sprite Engine
Address Control Logic

- Performs Memory Addressing Function for Build and Display Buffers

- Compositing Addressing
  - Address Broken into 2 Portions - I, J
  - One Address Per 4 Pixels in 1 x 4 Array
    - Addresses (8:0) - I location
    - Addresses (13:9) - J location
**Address Control Logic**

Normal Mode
Compositor and Display Address

A<09> = 0

A<09> = 1

Compositing and Display Addressing

(accesses the four different buffers simultaneously as a 1x4 array)
Media DAC

♦ Standard RGB Output
  • 135 MHz DACs
  • 1344 x 1024 at 75 Hz

♦ 3 x 256 x 8 Color LUTs
  • Loaded from Media DSP via Media Bus
Media Bus

♦ 16 Bit Multimedia Bus @ 40 MHz

♦ PCI - like Protocol

♦ Interface for Device Initialization and Operational Control of the Compositing DAC

♦ Expandable for future high performance interface for Additional MM Devices
Summary

♦ SRAM Based C-DAC Design Complete
♦ Large Chip for SRAM Design (~ 14mm x 14mm)
♦ Price Point Requirements Dictate DRAM Based Cell Design
♦ Next Step Design in Process