V830R/AV: Embedded Multimedia Superscalar RISC Processor with Rambus® Interface

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NEC Corporation

Outline

- Chip Highlights
- Instruction Set Architecture (ISA)
- Micro Architecture
- Performance
- Summary
Chip Highlights (1)

- High Performance Embedded RISC
  - Dual-issue Superscalar
  - 200MHz
  - Over 250 MIPS@Dhrystone 1.1
  - 2,000 MOPS@16-bit Data
    - MPEG2 A/V Decoding
    - MPEG1 Video Encoding
  - Under 2W Power Consumption

- 32KB On-chip Cache Memory
  - 16KB 4-way Instruction Cache
  - 16KB 4-way Non-blocking Data Cache
  - Freeze Function

Chip Highlights (2)

- Multimedia Extension
  - 64-bit SIMD Multimedia Coprocessor
  - Multimedia Oriented Peripheral Integration
    - Audio/Video Output Port

- On-chip Rambus DRAM Interface
  - High Bandwidth Rambus DRAM Memory System
  - Multimedia Processing in UMA Environment
  - Memory/System Separated Bus
    - Sufficient Bandwidth for Total System Operation

- On-Chip Debug Support
  - ICE Interface
Chip Highlights (3)

- **Technology**
  - 0.25\(\mu\)m CMOS
  - 4 Layer Metal
  - 2.5V with 3.3V I/O
  - 3M Tr.

- **Package**
  - 208-pin Plastic QFP
  - 0.5mm Lead Pitch

V830 ISA

- **RISC ISA with Improved Code Density**
  - Based on V810 RISC ISA
  - 32 General Purpose Register Set
  - Variable Length Code Format
    - 16-bit and 32-bit
  - 2-operand

- **MIX : Multimedia Instruction Extension**
  - Extension for Media Signal Processing
    - 32-bit Saturation Arithmetic Operation
    - 32-bit Pipelined Single-cycle MAC Operation
    - 32-bit Min/Max Operation
    - 32-bit Concatenate and Shift Operation
  - 3-operand
V830R ISA

- V830 Upward Compatible Integer ISA
- MIX2: Multimedia Instruction Extension 2
  - 64-bit SIMD Media Coprocessor
    - 32 Coprocessor Register Set
    - 56 SIMD Media Instructions
      - Saturated Additions
      - Saturated Subtractions
      - Multiply-and-Accumulate (MAC)
      - ME Oriented Special Instructions
    - 3-operand
  - Cache Control Instructions
    - Invalidate
    - Write Back

MIX2 Summary

<table>
<thead>
<tr>
<th>32-bit Transfer</th>
<th>64-bit Transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Move Mem. -&gt; CP Reg.</td>
<td>ldcp.w</td>
</tr>
<tr>
<td>CP Reg. -&gt; Mem.</td>
<td>stcp.w</td>
</tr>
<tr>
<td>Reg. -&gt; CP Reg.</td>
<td>mtcp.d</td>
</tr>
<tr>
<td>CP Reg. -&gt; CP Reg.</td>
<td>mfcph.w, mfcpl.w</td>
</tr>
<tr>
<td>CP Reg. -&gt; Mem.</td>
<td>movcp.d</td>
</tr>
</tbody>
</table>

- Arithmetic Vector Add: vsatadd.b, vadd.h, vsatadd.h, vadd.w
- Vector Subtract: vsatsub.b, vsub.h, vsatsub.h, vsub.w
- Vector Multiply: vmul.h, vmult.h
- Vector MAC: vmac.h, vmacr.h, xvmach.hw, xvmaccl.hw
- Scalar Add: sadd.h
- Scalar Subtract: ssub.h
- Scalar Multiply: smul.h, smult.h
- Scalar MAC: smac.h, smacr.h, smacr.h
- Compare Vector Max: vmx.h
- Vector Min: vmin.h
- Scalar Max: smax.h
- Scalar Min: smin.h
- Convert Pack: cvtpk.hb
- Interleave: itlvh.b, itlvl.b, itlvh.h, itlvl.h, itlvh.w, itlvl.w
- Logical OR: orcp.d
- AND: andcp.d
- XOR: xorcp.d
- Not: notcp.d
- Shift Logical Left: vshl.h, vshl.w, vshl.d
- Logical Right: vshr.h, vshr.w, vshr.d
- Arithmetic Right: vsar.h, vsar.w
- Shift and Add: vsftadd.hw, vsftadd.w
- Etc. Partial Absolute Diff: vpad.bh
Pipeline Structure

- **6-stage De-coupled Pipeline**
  - Instruction Pipeline is De-coupled with Execution Pipelines
  - High Frequency Operation

- **Instruction Pipeline (I-pipe)**
  - Early Resolution of Branch

- **Integer Pipeline (V-pipe)**
  - Data Forwarding

- **Media Pipeline (M-pipe)**
  - Multiple Execution Stages
  - No Data Forwarding

Superscalar Operation

- **Dual-issue Superscalar**
  - Media Instruction + Integer Instruction
  - In-order Issue
  - Out-of-order Completion

- **VLIW-like Instruction Issue**
  - “Templated” Instruction Issue Scheme

- **Dependency Control**
  - Within Instruction Queue

- **Simple Exception Handling**
  - No Exception on M-pipe
  - No Side-effect on V-pipe Exception
Instruction Unit

- Branch Prediction
  - 2-bit Branch Prediction Table
- Branch Target Address Cache
  - 128 Entries (64x2)
  - 2-way Set-associative
  - LRU Replacement
- Instruction Queue
  - 24-byte (Up to 12-instructions)
  - Squash Unconditional Branch
    - Zero Clock Branch
    - Conceal Overhead due to Variable Length Instruction Code
    - De-coupled Structure
  - “Templated” Instruction Issue Scheme

“Templated” Instruction Issue Scheme

VLIW-like Parallel Issue Template

M → V16
or
M → V32
Integer Unit

- 32 x 32-bit General Purpose Registers
- Conventional 4-stage Pipeline
  - RF, EX, DF, WB
  - With Data Forwarding Control
  - With Interlock Control
- Multimedia Oriented Function
  - 32-bit x 32-bit Multiply-adder
    - Precision required Signal Processing such as Audio Processing
    - Concatenate and Shift
      - Useful for VLC/VLD

Media Extension Unit

- 32 x 64-bit Coprocessor Registers
- 64-bit SIMD Datapath
  - Supported Data Type
    - 64-bit x 1, 32-bit x 2, 16-bit x 4 (Signed Integer, Signed Fixed Point), 8-bit x 8
  - SIMD Capability
    - 16-bit Multiply-adder with Special Rounding
    - Extended Precision MAC Operation
      - Dual 16-bit x 16-bit + 32-bit --> 32-bit MAC Operation
- Simple 4-stage Pipeline with Multiple Execution Stage
  - RF, EX1, EX2, WB
  - No Data Forwarding
    - Latency/Repeat = 4/1
  - No Exception
Special Rounding

- **Maximize Precision**
  - Fixed Point Style Data Handling
  - Used in vmacrs.h, smacrs.h Instruction

- **Rounding Scheme**
  - Decimal Point Adjustment
  - Symmetrical Rounding

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Precision Evaluation

- **IDCT Algorithm**
  - Row-Column Composed 2D-DCT
  - Double Stage Composed 1D-DCT

- **Evaluation Data**
  - Random
  - From -384 to 383

<table>
<thead>
<tr>
<th></th>
<th>PEAK ERROR</th>
<th>MEAN SQUARE ERRORS</th>
<th>MEAN ERRORS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Worst Overall</td>
<td>Worst Overall</td>
</tr>
<tr>
<td>IEEE1180 Upper Limit</td>
<td>1</td>
<td>0.0600 0.020000</td>
<td>0.0150 0.001500</td>
</tr>
<tr>
<td>Without Special Rounding</td>
<td>1</td>
<td>0.0791 0.060617</td>
<td>0.0061 0.000561</td>
</tr>
<tr>
<td>With Special Rounding</td>
<td>1</td>
<td>0.0122 0.010145</td>
<td>0.0026 0.000016</td>
</tr>
</tbody>
</table>
Cache Summary

<table>
<thead>
<tr>
<th></th>
<th>I-Cache</th>
<th>D-Cache</th>
</tr>
</thead>
<tbody>
<tr>
<td>Associativity</td>
<td>4-way Set Associative</td>
<td>4-way Set Associative</td>
</tr>
<tr>
<td>Replacement</td>
<td>LRU</td>
<td>LRU</td>
</tr>
<tr>
<td>Write Strategy</td>
<td>-</td>
<td>Write Back/Write Allocate</td>
</tr>
<tr>
<td>Non-Blocking</td>
<td>-</td>
<td>Hits under Miss</td>
</tr>
<tr>
<td>Capacity</td>
<td>16KB</td>
<td>16KB</td>
</tr>
<tr>
<td></td>
<td>Freezable upto 8KB on Entry Basis</td>
<td>Freezable upto 8KB on Entry Basis</td>
</tr>
<tr>
<td>Line Size</td>
<td>64B</td>
<td>64B</td>
</tr>
</tbody>
</table>

Cache Freeze Function

- Can be used as Ideal Memory
  - Never Miss
  - No Unpredictable Miss Penalty
  - Useful for Timing Assurance

- Freezing Scheme
  - Way-0 and Way-1
    - Up to 8KB can be Frozen
  - Entry by Entry Basis
    - Reduced Way Cache Operation

- On-demand Setup Capability
  - Load and Freeze at Initial Access Time
  - Don’t care for explicit Loading
**RCU : RDRAM™ Control Unit**

- **Concurrent RDRAM Protocol Support**
  - Lower Latency with DRAM State Management
  - Higher Transfer Data with Interleaved Access
  - Max. 18M-byte
    - Up to 8 16M/18M RDRAM
    - Up to 2 64M/72M RDRAM

- **Memory Request Queuing**
  - 8-entry Instruction Queue
  - 64-byte x 8 Data Buffer

- **Interleaved Access**
  - 128-byte = 2 x 64-byte
  - 256-byte = 4 x 64-byte

- **Pre-fetch**
  - In Case of I-Cache Refill
  - Next 64-byte

- **Address Re-mapping**
  - Utilize Sense-amp Cache
  - Avoid Bank Conflict

**RCU Structure**

Diagram showing the internal bus, Ibus slave-if, Command decoder, Scoreboard, Data buffer (64-byte 8-entries), Instruction queue (8-entries), RMC control, RMC, RAC, and RDRAMs (max. 8 devices).
Other Peripherals

- Multimedia Peripherals
  - VCU : Video Control Unit
    - 16-bit Video Output
    - Double Data Buffer (256-byte X 2)
    - Y1C/Y0Cb Pixel Data Format
  - ACU : Audio Control Unit
    - Serial Audio Output
    - Double Data Buffer (256-byte X 2)
    - 16b 2-channel Audio Data Format

- “Bulk” DMA Unit
  - Efficient “Packed” Data Transfer between
    - RDRAM and System Bus
    - RDRAM and Internal Peripherals
  - 4-ch

- Bus Control Unit
  - 32-bit A/D Multiplexed
  - Up to 66MHz
  - Single&Burst Bus Cycle

- Standard Peripherals
  - UART : 150~76800BPS
  - CSI : ~8.25MBPS
  - BRG
  - RPU : 16-bit Timer x 3
  - ICU : 17-ch
  - PORT : 1-bit I/O Port x 3

- Debug Control Unit
  - Serialized ICE Interface

- Standard Peripherals
  - UART : 150~76800BPS
  - CSI : ~8.25MBPS
  - BRG
  - RPU : 16-bit Timer x 3
  - ICU : 17-ch
  - PORT : 1-bit I/O Port x 3

Performance (1)

- MPEG2 A/V Decoding Profile
- Video
  - 720 x 480 x 30fps
  - 4:2:0 Format
  - 4Mbps
- Audio
  - MPEG Audio Layer2
- System
  - Program Stream Decode
Performance (2)

- MPEG1 Video Encoding Profile
- Search Range
  - +/- 16 Pixels
- 3 Step Search Algorithm
  - 2 x 2 Subsampling
  - Pel Precision
  - Half-Pel Precision
- Frame Structure
  - I2P8B20
  - 48fps

Summary

- High Performance Embedded Superscalar RISC Processor
  - Dual-issue Superscalar by VLIW-like “Templated” Instruction Issue Scheme
  - 32K-byte On-chip Cache Memory with Freeze Capability
  - 258MIPS, 2,000MOPS@16-bit at 200MHz

- 64-bit SIMD Multimedia Extension
  - Specially Designed 16-bit MAC with Special Rounding Scheme
  - 4-way Parallel IDCT Compliant to MPEG2 Standard

- On-chip Rambus® DRAM Interface
  - UMA for Multimedia Processing with 600MB/s Rambus DRAM Memory System
  - Realizes A Processor based Low Cost MPEG2 A/V Decoding System