Genesis
Microprocessor
Hot Chips X
August 17, 1998

Jack Choquette
Principal Engineer & Architect

SandCraft, Inc.
3003 Bunker Hill Lane
Suite #101
Santa Clara, CA
(V) 408.490.3237
(F) 408.490.3111
www.sandcraft.com
Presentation Outline

- Design Objectives
- Processor Features
- Micro-Architecture Overview
- Dual-Issue Superscalar Implementation
- Feature Comparison
- Summary
Design Objectives

- High Performance: 200+ MHz, 400 Dhrystone MIPS
- Efficient Memory: High Performance in Low Cost System
- Unique Features: DSP Functions & Image Processing
- Debug: System Debug Support
- Low Cost: 7mm x 7mm Die, Plastic Package
- Time To Market: 15 Months Development Time

Project Goal: Highest Performance in Its Class
Genesis Feature List

- **ISA:** MIPS-I through MIPS-IV, with Extensions to Support DSP & Vector Processing
- **Pipeline:** Symmetric Dual-Issue Superscalar
  - 2 Unified Integer-FP Units
  - Multiply-Accumulate Unit
  - 8 x 8-bit Packed-Data Vector Unit
  - Load-Store Unit
  - Branch Unit
- **I-Cache:** 32K-bytes, 2-way Set-Associative, Line Locking, LRU, Word Parity
- **D-Cache:** 32K-bytes, 2-way Set-Associative, Line Locking, LRU, Byte Parity, Write Back / Write Through
- **MMU:** 48 Double-entry Fully Associative TLB, with Separate 4-entry Micro TLB for Instruction & Data
- **Sys Interface:** R5000 Downward Compatible, with Features to Minimize Latency & Increase Throughput
- **Debug:** JTAG, N-Wire/N-Trace
Goals

DSP & Image Processing Support
Extended Instructions

- MIPS-IV ISA, Plus Following Enhancements:
  - 16 New Integer Multiply Accumulate Instructions
    - 32 x 32 Multiply with 64-bit Accumulate
    - 3 Cycle Latency, 1 Cycle Repeat Rate
  - 32-bit and 64-bit Rotate Instructions
  - 31 New Media Instructions
    - 8 x 8 bit Vector Instructions
    - Single 8 x 24-bit Vector Accumulator
    - Two or One Cycle Latency
    - 1 Cycle Repeat Rate for Most Instructions
Goals

- DSP & Image Processing Support
- Maintain Performance with an inexpensive memory system
Memory Latency Tolerance Features

- Large Caches
  - 32K I, 32K D
  - 2-Way
  - Per Line Locking

- Non-blocking Load/Store Unit
  - Up to 4 Data Prefetches
  - Up to 4 Non-blocking Loads or Stores

- Split Transaction System Interface
  - 4-entry Transaction Buffer
  - Up to 4 Outstanding Read Request
  - Interleaved Write Operations Between Read Request and Response
Goals

- DSP & Image Processing Support
- Maintain Performance with an inexpensive memory system
- Easy and Inexpensive System Debug to Decrease System Designer’s Time to Market
Debug Features

- Industry-standard Debug Support
- IEEE 1149.1 JTAG
- N-wire, N-trace
- Full External Access to:
  - Processor Architecture State
  - System Memory
- Multiple Breakpoints on:
  - Instruction Address
  - Data Address
  - Data Value
- Single-step Through Code
- Instruction Trace Capabilities and Performance Counters
Goals

- DSP & Image Processing Support
- Maintain Performance with an inexpensive memory system
- Easy and Inexpensive System Debug to Decrease System Designer’s Time to Market
- Clean and Efficient Microarchitecture
Micro-Architecture Block Diagram

IC Stage

RF Stage

EX Stage

DC Stage

WB Stage
Data Pipeline

Register File

Left Operands

Left Result

Load/Store Unit

MAcc/Vector Unit

Right Operands

Right Result

Left Int/FP Unit

Right Int/FP Unit

Left Result Staging

Right Result Staging

Left Pipe

Right Pipe
Genesis Microprocessor
# NEC VR5464™ Device Specification*

<table>
<thead>
<tr>
<th>Category</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.25um, 3LM, 6-T SRAM cells</td>
</tr>
<tr>
<td>Frequency</td>
<td>250 MHz Pipeline, 100 MHz I/O</td>
</tr>
<tr>
<td>Performance</td>
<td>519 MIPS, 10 SPECint95, 4.5 SPECfp95</td>
</tr>
<tr>
<td>Die Size with scribe</td>
<td>47 mm²</td>
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<tr>
<td>Voltage Supply</td>
<td>3.3-volt I/O, 2.5-volt Core</td>
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<tr>
<td>Power Consumption</td>
<td>4.4 watts</td>
</tr>
<tr>
<td>Package</td>
<td>272-pin plastic BGA</td>
</tr>
<tr>
<td>Price (10K)</td>
<td>$95</td>
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</tbody>
</table>

*Source: Microprocessor Report 3/9/98

TM -- trademark of NEC Electronics
### Feature Comparison

<table>
<thead>
<tr>
<th></th>
<th>VR5464</th>
<th>VR5432</th>
<th>RM5270</th>
<th>RM5230</th>
<th>EC603e</th>
<th>SA-110</th>
<th>SH7750</th>
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<tbody>
<tr>
<td><strong>Architecture</strong></td>
<td>MIPS</td>
<td>MIPS</td>
<td>MIPS</td>
<td>MIPS</td>
<td>PowerPC</td>
<td>ARM</td>
<td>SuperH</td>
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<tr>
<td><strong>Vendor</strong></td>
<td>NEC</td>
<td>NEC</td>
<td>QED</td>
<td>QED</td>
<td>Motorola</td>
<td>Intel</td>
<td>Hitachi</td>
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<tr>
<td><strong>IP Provider</strong></td>
<td>SandCraft</td>
<td>SandCraft</td>
<td>QED</td>
<td>QED</td>
<td>Motorola</td>
<td>Digital</td>
<td>Hitachi</td>
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<td><strong>Frequency</strong></td>
<td>250 MHz</td>
<td>167 MHz</td>
<td>200 MHz</td>
<td>175 MHz</td>
<td>266 MHz</td>
<td>233 MHz</td>
<td>200 MHz</td>
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<td><strong>Execution Units</strong></td>
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<td>6</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>2</td>
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<tr>
<td><strong>Issue/clock</strong></td>
<td>2</td>
<td>2</td>
<td>1 Int, 1 FP</td>
<td>1 Int, 1 FP</td>
<td>2</td>
<td>1</td>
<td>2</td>
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<tr>
<td><strong>FPU?</strong></td>
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<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>no</td>
<td>no</td>
<td>yes</td>
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<tr>
<td><strong>Hardware MAC?</strong></td>
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<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
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<tr>
<td><strong>Vector operations?</strong></td>
<td>yes</td>
<td>yes</td>
<td>no</td>
<td>no</td>
<td>no</td>
<td>no</td>
<td>yes</td>
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<tr>
<td><strong>Caches (I/D)</strong></td>
<td>32K / 32K</td>
<td>32K / 32K</td>
<td>16K / 16K</td>
<td>16K / 16K</td>
<td>16K / 16K</td>
<td>16K / 16K</td>
<td>8K / 16K</td>
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<tr>
<td><strong>Non-blocking Load/Stores</strong></td>
<td>yes</td>
<td>yes</td>
<td>no</td>
<td>no</td>
<td>no</td>
<td>no</td>
<td>no</td>
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<td><strong>Cache locking?</strong></td>
<td>yes (per line)</td>
<td>yes (per line)</td>
<td>yes (per set)</td>
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<td>no</td>
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<td><strong>Bus width</strong></td>
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<td>64 bits</td>
<td>64 bits</td>
<td>32 bits</td>
<td>64 bits</td>
<td>32 bits</td>
<td>64 bits</td>
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<td><strong>IEEE 1149.1 JTAG support?</strong></td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>?</td>
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<td><strong>Debug support?</strong></td>
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<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
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<tr>
<td><strong>Fab process / Metal Layers</strong></td>
<td>0.25um / 3LM</td>
<td>0.25um / 3LM</td>
<td>0.35um / 3LM</td>
<td>0.35um / 3LM</td>
<td>0.35um / 4LM</td>
<td>0.35um / 3LM</td>
<td>0.25um</td>
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<td><strong>Die Size</strong></td>
<td>47 mm²</td>
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<tr>
<td><strong>Voltage (V)</strong></td>
<td>2.5 / 3.3</td>
<td>2.5 / 3.3</td>
<td>3.3V</td>
<td>3.3</td>
<td>2.5 / 3.3</td>
<td>1.65 / 3.3</td>
<td>1.8 / 3.3</td>
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<td><strong>Power (typical)</strong></td>
<td>4.4W</td>
<td>2.5W</td>
<td>4.0W</td>
<td>3.6W</td>
<td>4.8 W</td>
<td>1.1W</td>
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<td><strong>Dhrystone MIPS</strong></td>
<td>519</td>
<td>347</td>
<td>260</td>
<td>227</td>
<td>376</td>
<td>268</td>
<td>360</td>
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<td><strong>MIPS/MHz</strong></td>
<td>2.1</td>
<td>2.1</td>
<td>1.3</td>
<td>1.3</td>
<td>1.4</td>
<td>1.2</td>
<td>1.8</td>
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<td><strong>SPECint95</strong></td>
<td>10 (est.)</td>
<td>n/a</td>
<td>5.5</td>
<td>4</td>
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<td><strong>SPECfp95</strong></td>
<td>4.5 (est.)</td>
<td>n/a</td>
<td>6.1</td>
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Conclusion

Project Goals Emphasized:

- Design Efficiency and High Execution Throughput
  - De-coupled Instruction Fetch and Execution Datapaths
  - Symmetric Dual Pipelines
  - DSP & Image Processing Extensions
- Low Cost without Sacrificing Performance
  - Efficient Memory
  - Clean Superscalar implementation
  - Inexpensive Processor
  - Debug Support for Faster System Design
- Making a Clean Design to Achieve the Shortest Development Time
  - From Specification to Tapeout in 15-1/2 Months

Full Featured, Desktop Performance, Embedded Price