A Single Chip DTV Media Processor

Selliah Rathnam

Philips Semiconductors

Trimedia - DTV
Trimedia CPU Generations

• **TM-1000: 100 MHz VLIW CPU**
  – Co-processors: VLD, ICP
  – Silicon Status: In production

• **TM-1100: 133MHz VLIW CPU**
  – New Co-processor/Bus: DVD de-scrambler/PCI-XIO
  – CPU Enhancement: six new operations to enhance CPU power
  – Silicon Status: Sampling now
Trimedia CPU Generations (Cont’d)

- TM-2 (DTV): Single chip DTV media processor
  - Major new/modified Co-processors:
    - Slice-level MPEG2 video decoder
    - High definition video display pipe (HDVO)
  - Concurrent SPDIF audio output
  - 64-bit memory interface
Key DTV Set Functions

- **Transport Demux**
- **MP@HL all 18 resolution video decoding**
- **AC-3 or MPEG audio decoding**
  - AC-3 5.1ch@384Kbps and 2ch@192Kbps
- **2D,3D graphics generation (GUI, browser, ...)**
- **Display chain (scaling H&V, alpha blending, chroma keying, de-interlacing)**
- **PIP, Closed Caption decode**
- **Modem**
Optional DTV Functions

- Decode discretionary format (Datacasting etc.)
- Improved rendering of NTSC (Natural motion etc.)
- Browser and push content display
- Video conferencing (with external camera)
- Mid performance 3D (VRML, games)
**Defining the ATSC Standard**

**ATSC specification optional standards for DTV**

All 18 formats refer to input and output configurations.

<table>
<thead>
<tr>
<th></th>
<th>vertical lines</th>
<th>pixels</th>
<th>aspect ratios</th>
<th>picture</th>
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</thead>
<tbody>
<tr>
<td><strong>HDTV</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1080</td>
<td>1920</td>
<td>16:9</td>
<td>60I, 30P, 24P</td>
<td></td>
</tr>
<tr>
<td>720</td>
<td>1280</td>
<td>16:9</td>
<td>60P, 30P, 24P</td>
<td></td>
</tr>
<tr>
<td><strong>SDTV</strong></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>480</td>
<td>704</td>
<td>16:9, 4:3</td>
<td>60P, 60I, 30P, 24P</td>
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</tr>
<tr>
<td>480</td>
<td>640</td>
<td>4:3</td>
<td>60P, 60I, 30P, 24P</td>
<td></td>
</tr>
</tbody>
</table>

Source: ATSC
**CPU block diagram**

- **Register file**: (128 32 bit registers)
  - 10+5 read ports
  - 5 write ports

- **Instruction cache**

- **SDRAM**

- **Instruction issue register**
  - five issue slots

- **Functional units**:
  - Functional unit 1
  - Functional unit 2
  - Functional unit 26
  - Functional unit 27

- **Issue slots**: Issue slot 1, Issue slot 2, Issue slot 3, Issue slot 4, Issue slot 5

- **Read & write crossbar**
## CPU Functional Units

<table>
<thead>
<tr>
<th>Functional Unit</th>
<th>Quantity</th>
<th>Latency</th>
<th>Recovery Time</th>
</tr>
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<tbody>
<tr>
<td>constant</td>
<td>5</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>integer ALU</td>
<td>5</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>load/store</td>
<td>2</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>DSP ALU</td>
<td>2</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>DSP MUL</td>
<td>2</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>shifter</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>branch</td>
<td>3</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>int/float mul</td>
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<td>3</td>
<td>1</td>
</tr>
<tr>
<td>float ALU</td>
<td>2</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>float compare</td>
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<td>1</td>
<td>1</td>
</tr>
<tr>
<td>float sqrt/div</td>
<td>1</td>
<td>17</td>
<td>16</td>
</tr>
</tbody>
</table>
DTV Single Chip System IC

- ATSC TS/CCIR 601 NTSC/PAL
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- Audio Sources
- Audio Sources
- I2C Master or Slave

- Video In #1
- Video In #2
- Audio In #1
- Audio In #2
- DMPC

- TM2 VLIW Core
- Ext Mem Interface
- Flexible MP@HL Accelerator
- XIO or PCI Bus
- HD Video Out
- SD Video Out
- SSI
- Audio Out
- DVD Support

- All 18 ATSC Formats
- CCIR601 Resolution
- To Modem FAE
- Four I2S for Surround
- One I2S for Headphones
- SP/DIF

Audio Sources

Philips Semiconductors
Key Features of TM2 based DTV System

- **Audio Output**
  - 6-ch main audio; 2-ch stereo for VCR; 2-ch stereo for PIP audio;
    - 20-bit Dolby digital compliance
  - Concurrent SPDIF output of main audio

- **Audio Input**
  - Two audio ports (IIS interface); receives PCM or SPDIF data through external glue logic
Key Features of TM2 based DTV System (Cont’d)

- Video-In
  - Two video-in units in order to receive two NTSC channels

- Transport Stream Input Unit
  - PID filtering in HW in order to reduce the CPU load for the ATSC demux function
  - Remaining demux functions are implemented in software
  - Shares the video-in pins
  - Two transport stream input units
Key Features of TM2 based DTV System (Cont'd)

- Video Out
  - High Definition Video out rgb 10-bit each
    - HD capable: 1920X1080 @ I60 fields/Sec or P30 frames/Sec, 74 Mpixels/Sec
    - Arbitrary Hor. And Vertical scaling,
    - PIP window, VCR output of main video
    - Graphics overlay
    - Aspect ratio conversion, interlacing, de-interlacing
  - Standard definition video-out in CCIR 656 format
  - Used for VCR recording
Key Features of TM2 based DTV System (Cont’d)

• MPEG2 co-processor for slice-level decoder
  – Capable of decoding MP@HL video bitstream
  – 2:1 compression mode in order to save memory
  – Error concealment in order to re-construct the region of image lost due to bitstream errors
Key Features of TM2 based DTV System (Cont’d)

- Memory/Hwy
  - 64-bit main memory interface
  - 64-bit Hwy for MPEG2 and HDVO; 32-bit highway for the remaining units
  - 2D read/write from MPEG2 co-processor
  - Supports 4Mbytes to 64 Mbytes of main SDRAM memory
**MPEG-Pipe**

- **Highway-32**
  - ATSC BW: 19.4 Mbits/Sec
  - Target: ~ 1 RL/Cycle
  - 2 coeff/Cycle

- **VLD**

- **Highway-64**
  - Worst Case BW: ~ 500 Mbytes/Sec
  - Optional 2:1
  - Error Concealment
  - 8 elements/Cycle

- **MC**

- **RL-ISCAN**

- **IQ**
  - 2 coeff/Cycle

- **IDCT**
TM2 Broadcast PIPs

HDTV Broadcast

NTSC/PAL Broadcast

OSD

HBO 7:43pm Dec 14th
Reminder: Harry's Birthday Next Week
**NTSC Movie**

- Fifty percent of Program content originates from movie
- Movie frame rate is 24 frames/sec (48 field/sec)
  - NTSC is 60 fields/sec
- One field is repeated for every four fields in order to show a movie in NTSC TV
  - Field repetition causes jerkiness in the objects in motion (≈ Eye strain)
NTSC Movie Display Improvements

- Natural motion algorithm has been developed in order to generate new (in-between) frames
  - 24 frames/sec => 60 frames/sec or 60 fields/sec
  - The result is a smooth motion while watching movies

- Natural motion algorithm will run in TM-2 CPU

- The SD resolution movie will be optionally scaled to HD display using high quality Hor. And vertical polyphase filters
Summary

• TM2000: high performance DTV media processing chip
  – Includes MP@HL video decode

• Status: Silicon will be sampled in 4Q 1998

• Project Experience:
  – Display processing consumes a significant amount of chip area
  – It is an exiting experience to work with HD video and AC-3 audio based DTV project
Thank you
Selliah Rathnam