Two Chipsets for DTV

Compliant with ATSC Standard

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Introduction

- 1st & 2nd generation chipsets compatible with ATSC

DTV

- standard

- Support 5 VSB modes: Terrestrial 8VSB and MMDS
- 2/4/8/16 VSB
- Transport demux having 16 bits interface with MCU
- MPEG2 MP@HL Video decoding including all 18 ATSC formats
- Video format conversion, any transmission to HD(1080I, 1st gen.) or SD(480I/P, 2nd gen.) display

- Seamless image format change
Chipset partitions

1st Generation Chipset Partition (5 chips, HD)

- Tuner
- I/F Demod. LA7785M
- ADC
- VSB
  - Channel Decoder (GDC21D002)
- Sync/EQ (GDC21D001)
- Transport (GDC21D301)
- 4M bit DRAM
- 8M Byte SDRAM
- Video Decoder (GDC21D401)
- Audio Decoder
- Mux
- MCU
- VDP (GDC21D701B)
- RGB/YCbCr
- 1080i
- 5.1 Ch. Audio

Diagrams and illustrations:

- DTV
- 1st Generation Chipset Partition (5 chips, HD)
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Chipset partitions

2. 2nd Generation Chipset Partition (2 chips, SD)

- DTV
  - Tuner
  - I/F Demod. (LA7785M)
- VSB Receiver (GDC21D003)
  - ADC
  - Sync
  - Equalizer
  - FEC
- 8M Byte SDRAM
- SD Video (GDC21S801)
  - Demux
  - MP@HL Dec.
  - VDP
  - Graphic Proce.
  - NTSC Enc./Dec.
  - D/A
- NTSC (Decoded /Not decoded)
- VGA (Analog)
- Audio Decoder
- Audio
- 5.1 Ch.
- RGB/YCbCr
- CVBS/S-Video
- 480I/P
- NTSC (Decoded/Not decoded)
- MC

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## Features of Video Chips

<table>
<thead>
<tr>
<th><strong>TP Decoder (1st Gen.)</strong></th>
<th><strong>Video Decoder (1st Gen.)</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>- Byte-parallel/bit-serial MPEG-2 TS input</td>
<td>- Decodable 18 input formats of ATSC standard</td>
</tr>
<tr>
<td>- Audio PES/Video ES output</td>
<td>- Tricky mode decoding</td>
</tr>
<tr>
<td>- Identify 32 PIDs</td>
<td>- MB 4 pixel parallel output</td>
</tr>
<tr>
<td>- Extract DTS/PTS for video decoder</td>
<td>- Decoding operation up to 54MHz</td>
</tr>
<tr>
<td>- PCR recovery</td>
<td>- 64bit Bus Mem. I/F (Four 1Mx16 SDRAM)</td>
</tr>
<tr>
<td>- Error code insertion for video</td>
<td>- Up to 81MHz async. Memory I/F</td>
</tr>
<tr>
<td>- 8/16-bit bus host interface</td>
<td></td>
</tr>
<tr>
<td>- Max. TS input rate: 80Mbit/s</td>
<td></td>
</tr>
</tbody>
</table>
Features of Video Chips

- Video Display Processor (1st Gen.)
  - 18 ATSC formats, 480x768I/P (NTSC), 480x640P, 768x1024P (SVGA) input
  - Analog/digital 1080 RGB/YCbCr output
  - De-interlacing using 3 field memory for 480I input
  - 9-tap horizontal peaking filter
  - PIP/Multi-PIP/Zoom
  - 2/4/16/256-colors/4-pixels OSD
  - RGB/YCbCr Color Space Converter
  - 8-bit custom controlled LUT
  - Host I/F: 16 bit parallel or I²C I/F

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Features of Video Chips

Features of SD Video (2nd Gen.)

- One-chip for TP, VD, VDP & NTSC
- MPEG2-TS/PES, DVD, DSS-SD(HD), Input picture formats: 18 ATS & MPEG-1 Decoding up to 100 Mbps
- EPG/SI(PAT, PMT, PSIP, etc) section filtering and CRC checking
- Identify 32 packet PIDs/table IDs
- PCR recovery
- PES layer audio output
- Down Conversion for HD stream
- Slice-based error concealment

Tricky mode decoding

Output picture formats:
Analog RGB/YCbCr/CVBS/S-Video & Digital 480x852I/P, 480x768I/P

3-D de-interlacing using 3 field memory for 480I input
Features of Video Chips

Features of SD Video (2nd Gen.)

- Seamless image format change
- PIP/Multi-PIP/Zoom/D-window
- 4 layer full screen bit-map OSD (2/4/8 bits color or 8 bits blending)
- NTSC Decoder/Encoder
- Fully compatible with EIA-608 NTSC closed caption
- Analog VGA Interface (4:4:4)
  - 3-channel 10-bit A/D
  - RGB to YCbCr Color Space Converter
- Max. 600 Mbits/s bandwidth at VGA main, DTV PIP, Dual prime decoding, and full screen OSD
- Video contents protection (V-chip)
- 16 bits host interface
- 8MB SDRAM interface
- No dead-lock condition
- Boundary scan test (JTAG)
- 0.35μm /3.3V/352BGA

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Features of Video Chips

Block Diagram of SD Video (2nd Gen.)

- AC-3 (main)/MPEG/PCM Audio PES Output
- AC-3 (Association) Data
- NTSC Input CVBS/S-Video/YUV
- Analog Outputs RGB/YPbPr/CVBS/S-Video
- Digital Output RGB/YCbcCr
- Memory Bus
- Host Bus
- Address Bus
- TPS Stream (IEEE1394)
- TP Stream (IEEE1394) to External Host Processor
- 8MB SDRAM (16Mbit * 4)
- ADA VGA RGB Input

Legend:

- Memory Bus
- Host Bus
- Address Bus
- In/Out Signals

DEGEND

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Features of VSB Chips

- Sync/Eq (1st Gen.)
  - Coherent & non-coherent AGC
  - DC reduction
  - Timing recovery
  - Data segment sync and Frame sync recovery
  - NTSC rejection comb filter
  - Decision-feedback equalizer
  - 64 tap FF & 192 tap FB Filter
  - Phase corrector

- VSB Ch. Dec. (1st Gen.)
  - 4&8 states TCM decoder: L=16
  - Slice prediction for phase corrector
  - De-interleaver
  - Reed-Solomon decoder (208,188)
  - Error flag insertion on erroneous packet
  - Tri-state parallel/serial MPEG-2 transport I/F
  - Internal segment error counter
Features of VSB Chips

Features of 1 Chip VSB Receiver (2nd Gen.)

- 10 bits differential ADC (1 Vpp)
- Coherent & non-coherent AGC
- Modified DS/Frame sync recovery
- Auto NTSC rejection comb filter
- Enhanced VSB mode detector
- Decision-feedback and
- Blind (D-D mode) Equalizer
- 64 tap FF & 192 tap FB Filter
- Concurrent coefficients updating
- Monitoring equalizer coefficients

- Intelligent loop controlled
- Phase Corrector
- 4&8 states TCM decoder : L=16
- Error flag insertion on error
- Tri-state parallel MPEG-2 TP I/F
- Internal segment error counter
- I²C bus Interface
- 0.35µm /3.3V
- 128pin HQFP
Features of VSB Chips

Block Diagram of 1 Chip VSB Receiver (2nd Gen.)

- Analog Input
- Digital Input (10 bits)
- DC Reduct.
- Polarity Correct.
- Comb Filter
- Channel Equalizer (256 taps)
- VSB mode Detector
- Phase Corrector
- Transport I/F
- Data De-randomizer
- Convolution De-interleaver
- Reed-Solomon Decoder
- Viterbi Decoder
- To Transport Decoder
- From VCXO
- To PLL
- P2C bus
- P2C Interface
- Clock Divider
- Timing Recovery
- DS Sync Recovery
- Field Sync Recovery
- To I/F
- To PLL
- Polarity Detect
- AGC
- ADC
- Mux
- Transport I/F
Design Methodology

- VHDL description
  - Summit, VI

- VHDL simulation
  - VSIM, leapfrog

- VHDL synthesis
  - Compass(Synopsys)

- Test Logic insertion
  - Compass(Synopsys)

- Gate level function & timing simulation
  - Compass(Synopsys)

- Place & route
  - Compass(Verilog-XL, VSIM)

- Layout verification
  - Compass(Verilog-XL, VSIM)

- H/W Emulation
  - Quikturn
  - Altera

- Real time test
  - 1st gen.(2nd gen.)

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## Implementation of 1st Gen. Chipset

### Summary of 1st gen. chipset implementation

<table>
<thead>
<tr>
<th>Chips</th>
<th>TP</th>
<th>VD</th>
<th>VDP</th>
<th>Sync/Eq</th>
<th>VCD</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Die size</strong></td>
<td>6x6</td>
<td>13x12</td>
<td>9x9</td>
<td>12x12</td>
<td>10x9</td>
</tr>
<tr>
<td><strong>Gate count (k)</strong></td>
<td>50</td>
<td>250</td>
<td>520</td>
<td>230</td>
<td>200</td>
</tr>
<tr>
<td><strong>Clock (MHz)</strong></td>
<td>27</td>
<td>54, 81</td>
<td>54, 65, 75</td>
<td>10.76</td>
<td>10.76</td>
</tr>
<tr>
<td><strong>Power (mW)</strong></td>
<td>300</td>
<td>1500</td>
<td>3000</td>
<td>2500</td>
<td>500</td>
</tr>
<tr>
<td><strong>Fab.</strong></td>
<td>LGS</td>
<td>LGS</td>
<td>LGS</td>
<td>LGS</td>
<td>LGS</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>0.6u, TLM</td>
<td>0.6u, TLM</td>
<td>0.35u, TLM</td>
<td>0.6u, TLM</td>
<td>0.6u, TLM</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>176 TQFP</td>
<td>240 HQFP</td>
<td>304 PQ2</td>
<td>160 PQ2</td>
<td>100 MQFP</td>
</tr>
<tr>
<td><strong>Status</strong></td>
<td>Q. S.</td>
<td>Q. S.</td>
<td>Revision</td>
<td>Q. S.</td>
<td>Q. S.</td>
</tr>
</tbody>
</table>
Implementation of 1st Gen. Chipset

- **Layout of 1st Gen Chipset**
  - **TP Demux**
  - **Video Decoder**
  - **VDP**
  - **Sync/Eq**
  - **VCD**
DTV Evaluation Board

- RGB out
- SDRAMs
- VDP
- VD
- ADC
- Demod.
- Tuner
- Transport
- VCD
- Sync EQ
- Timing recovery
- CPU MC68360
Conclusions

Implemented chipsets compliant with ATSC DTV transmission and video standard.

Multiple system functions were included on chip to reduce ultimate system cost.

Cost effective design using state-of-the-art ASIC technology is necessary to be supplied for consumer market.

Overlapping and intensive design verification should be done to get successful chip functioning for large gate-sized chips.